



HOW THINGS WORK

build kits · khanin.info

Building instructions

HT-01

The Payment Card

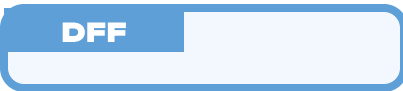
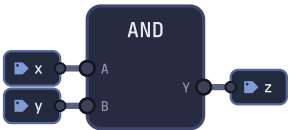
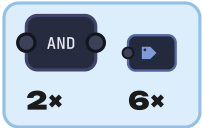
lessons 0-8 · a computer in the little gold square



simulator: cs.khanin.info

How to read these instructions

3



step number – follow strictly in order

parts for this step: how many to place

a part with labels on its pins

labels with the same name are connected

chip ports: input [and output]

blue frame – building a chip

grey tab – the main canvas

yellow ring – what has changed

remove a part together with its labels

double-click a label – new name

chip built in the lesson with this number

check: this is how it should work

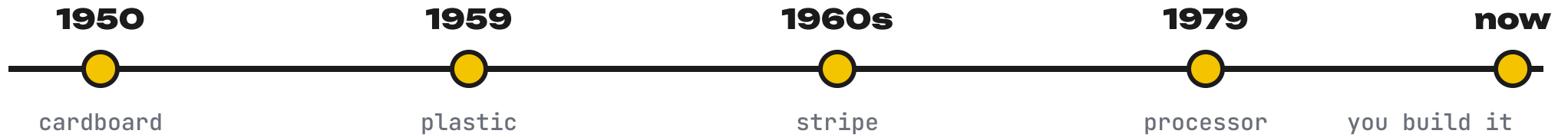
Keys

V	VCC (1)
G	GND (0)
N	transistor
I	switch
O	lamp
L	label
K	clock
U	button
[	port in
]	port out

Ctrl+G – into a chip
on a Mac Ctrl = Cmd



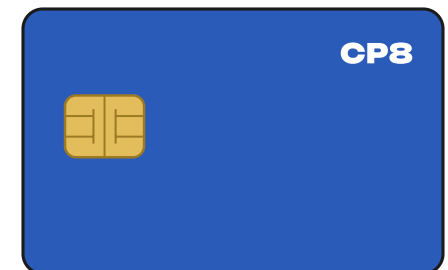
A little history



In 1950 Diners Club issued the first cards – made of cardboard. In 1959 cards became plastic, and the number was embossed: the merchant rolled the card through an imprinter and got a print on a paper slip.

In the late 1960s IBM put a magnetic stripe on the card – now a machine could read the number. But a stripe is easy to copy: it only stores a number, it does not think.

In 1979 Bull made the CP8 – a card with a processor, memory and a program. Since then the card never shows its secret: it answers the terminal's challenge. That is the computer you are going to build.



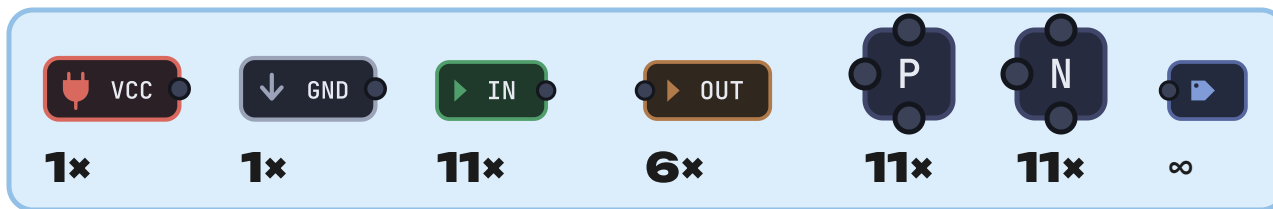
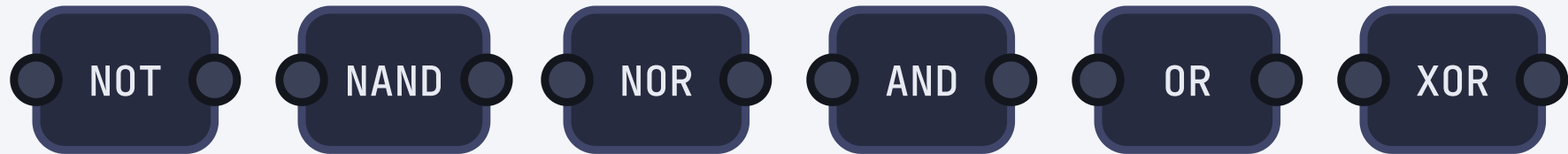
Diners Club, IBM, Bull are trademarks of their respective owners. This kit is not affiliated with or endorsed by them; the names are mentioned to tell the story.



Gates (optional)

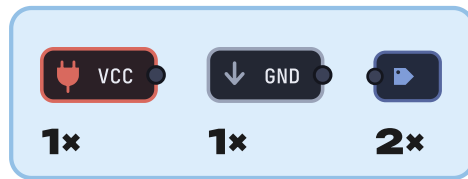
kh HT-01

NOT, NAND, NOR, AND, OR, XOR from transistors



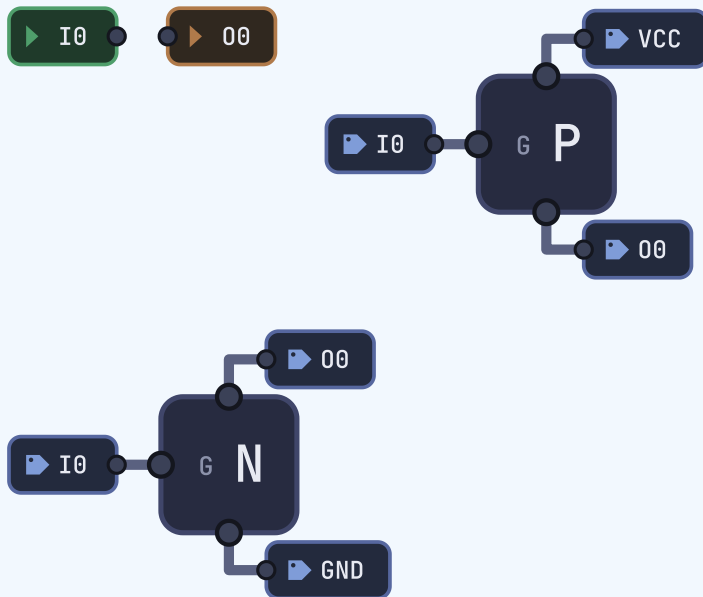
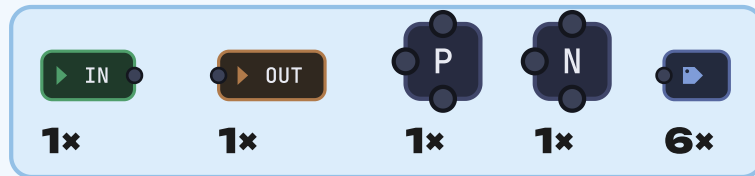
CANVAS

1



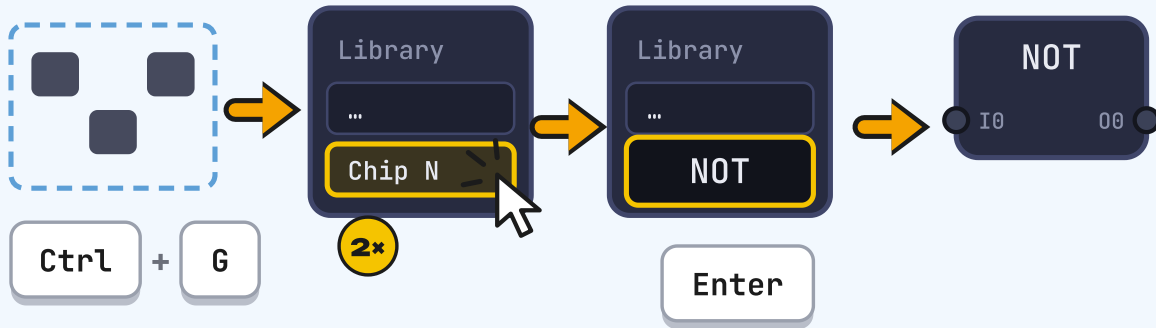
NOT

2



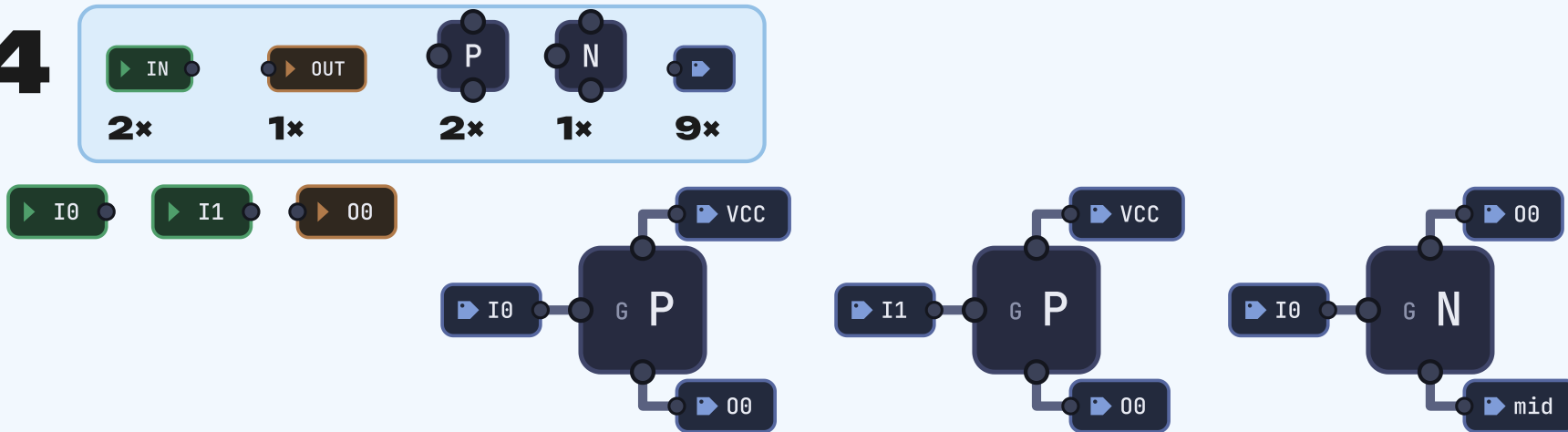
NOT ...

3



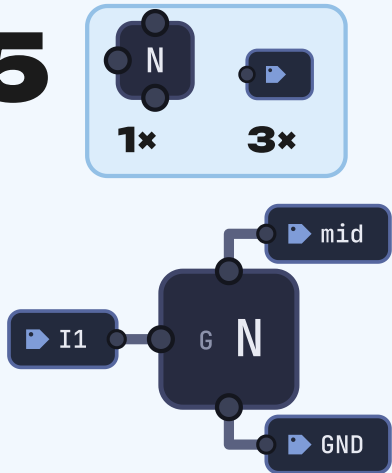
NAND

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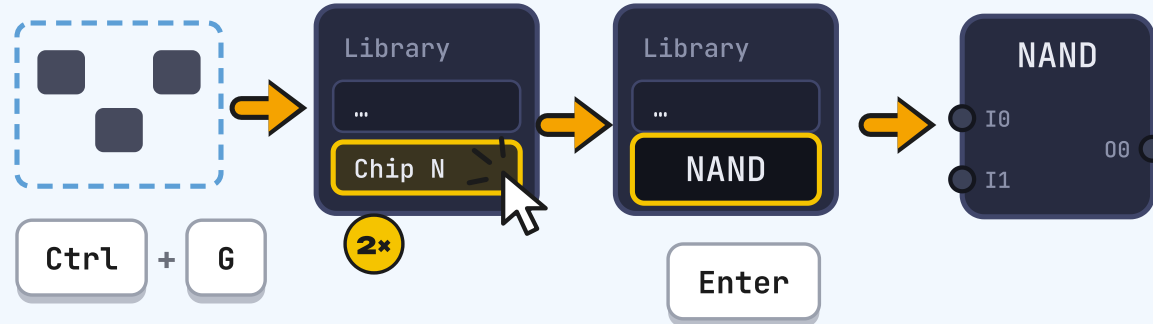


NAND ...

5

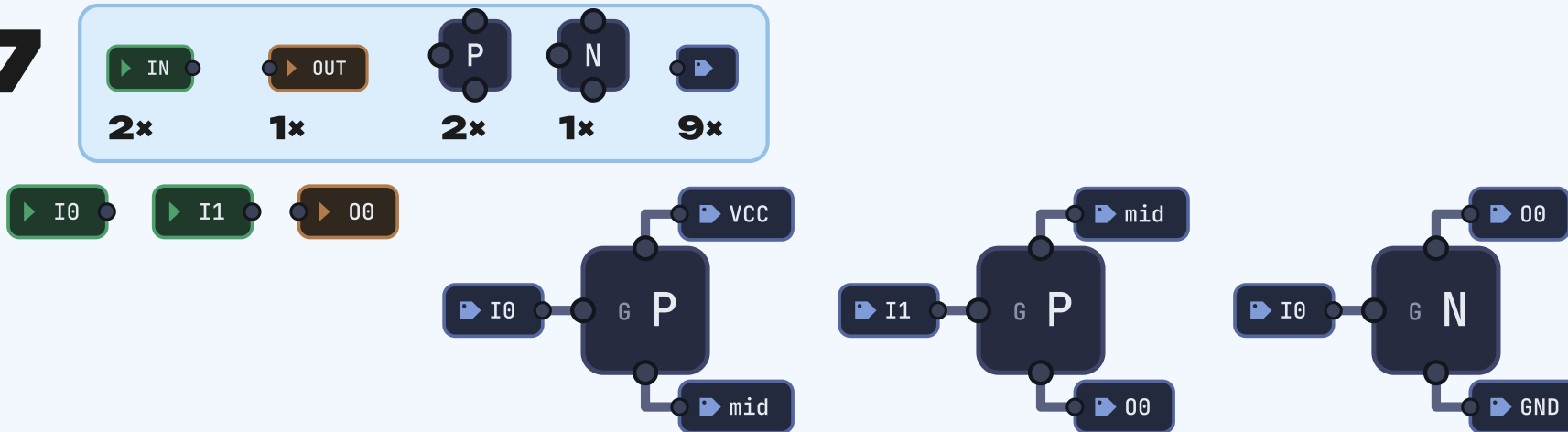


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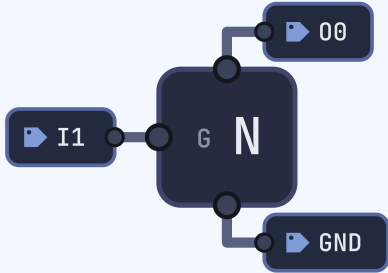
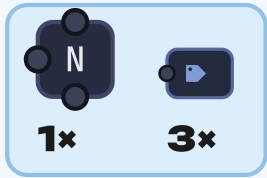
NOR

7

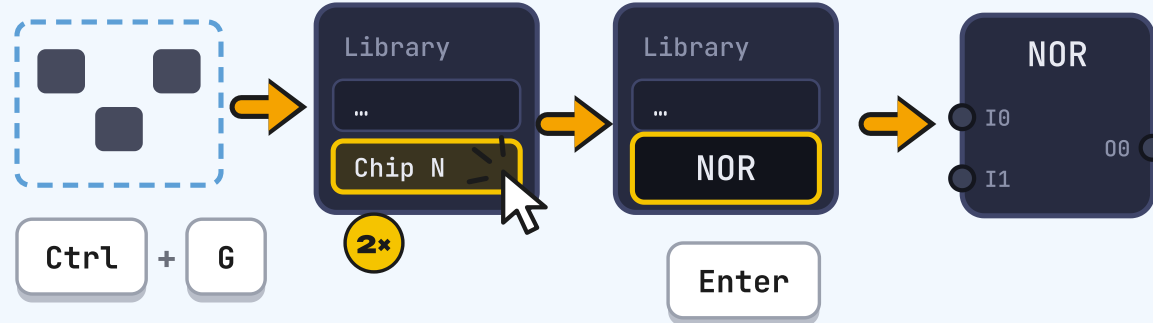


NOR ...

8

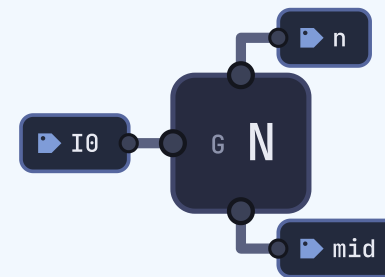
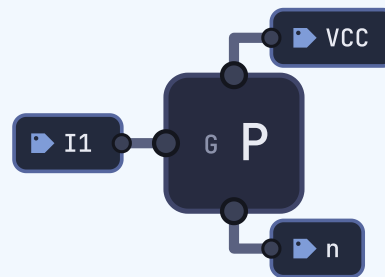
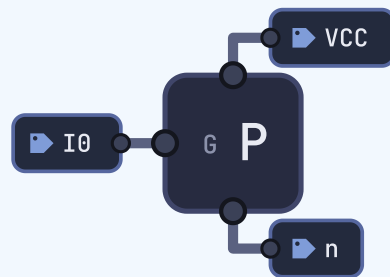


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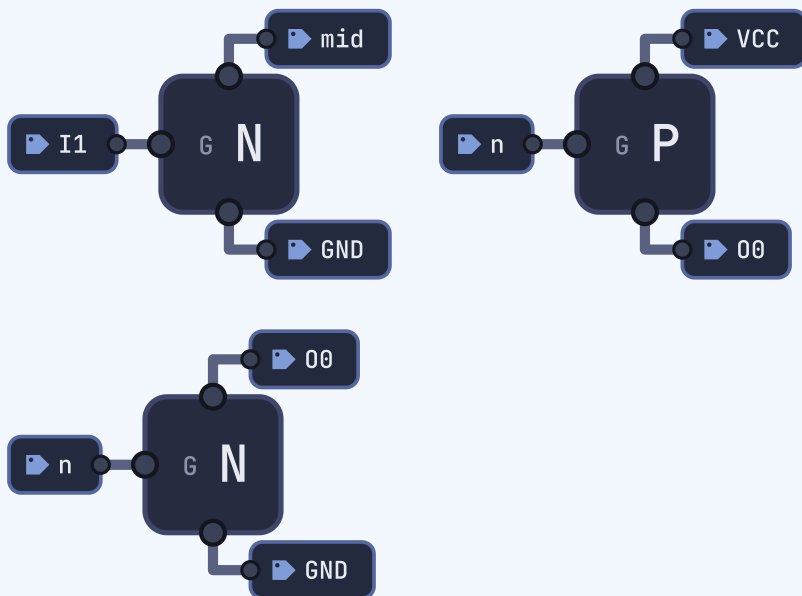
AND

10

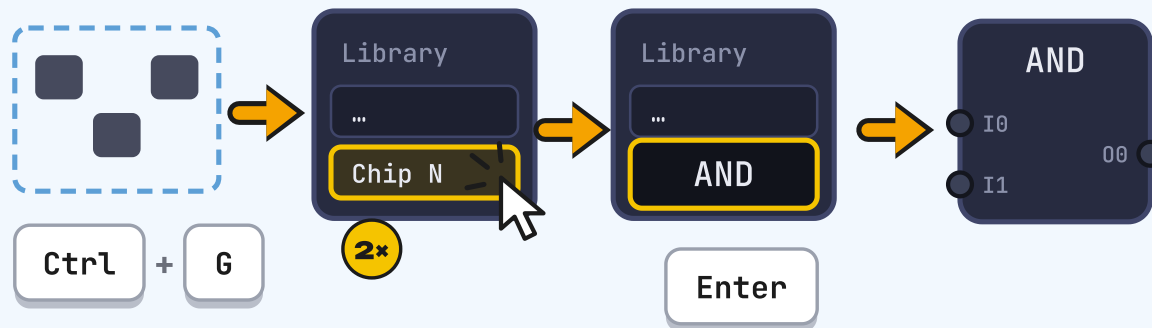


AND ...

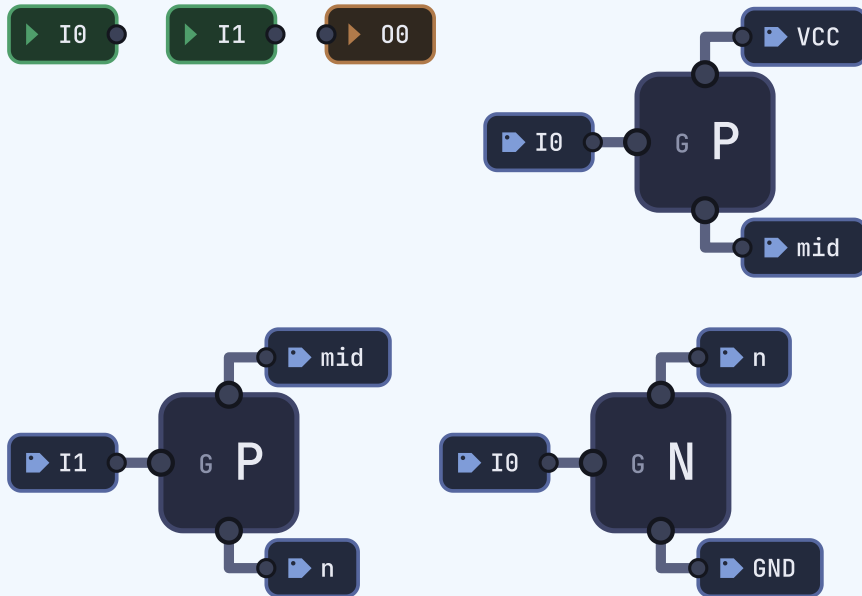
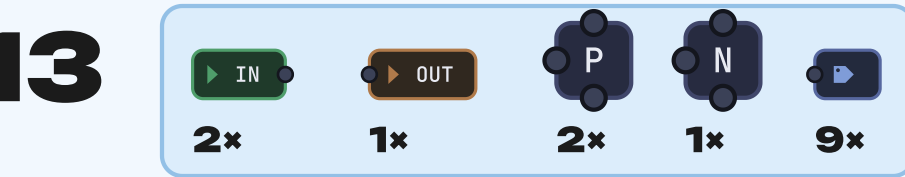
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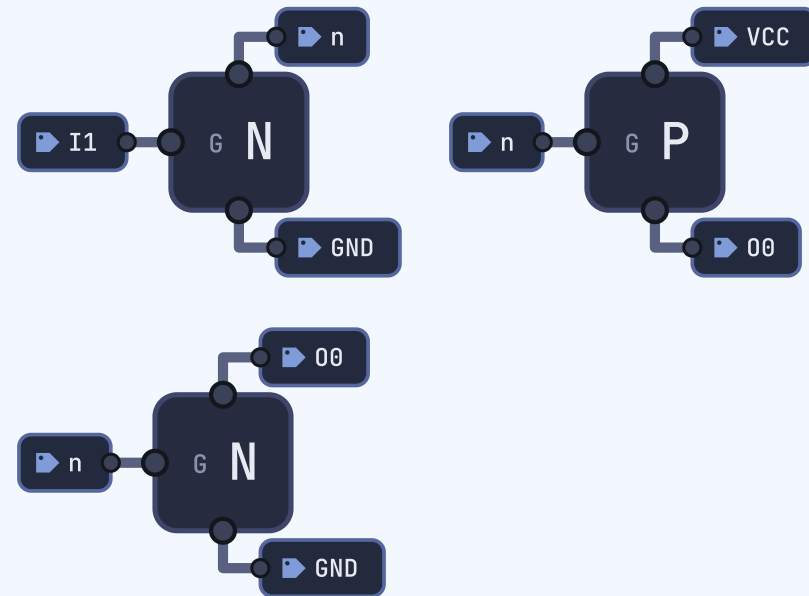
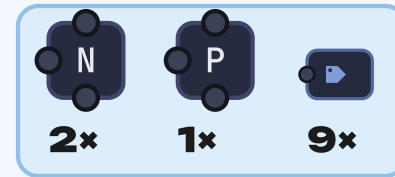
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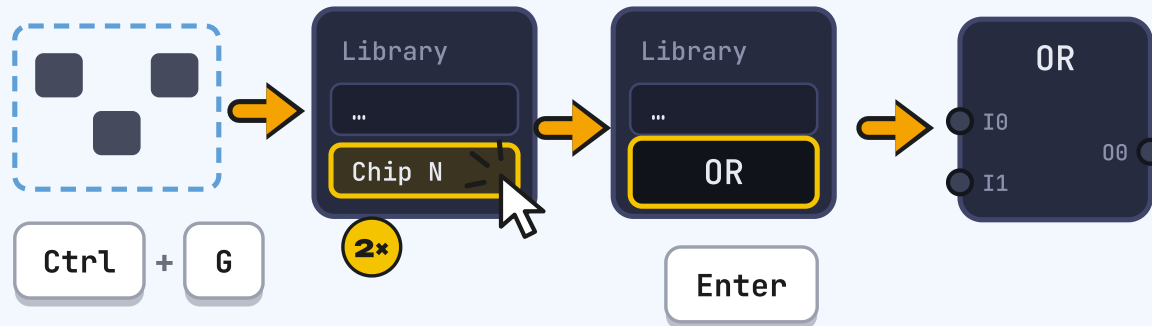
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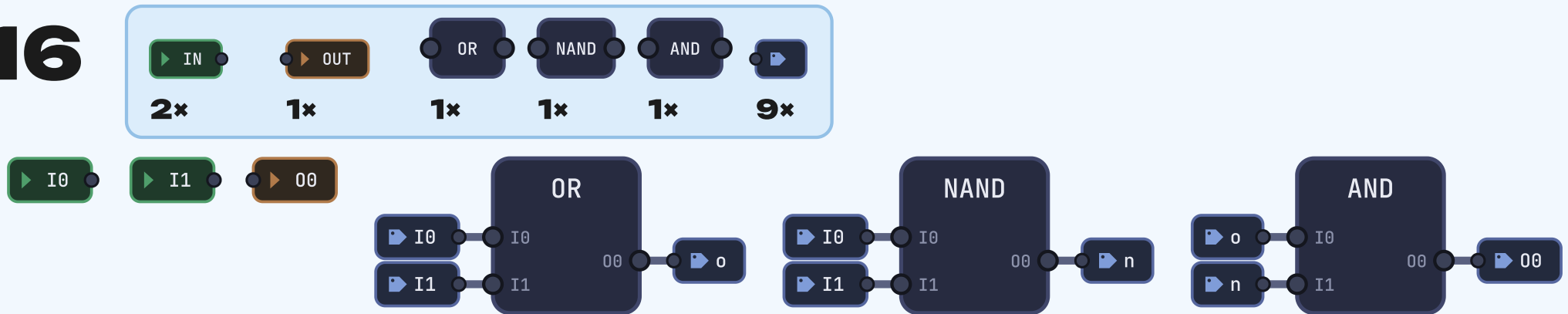


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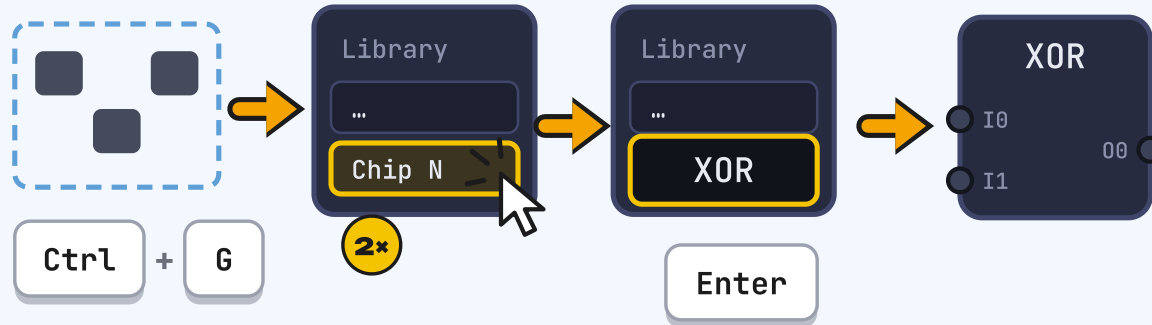


XOR

16



17

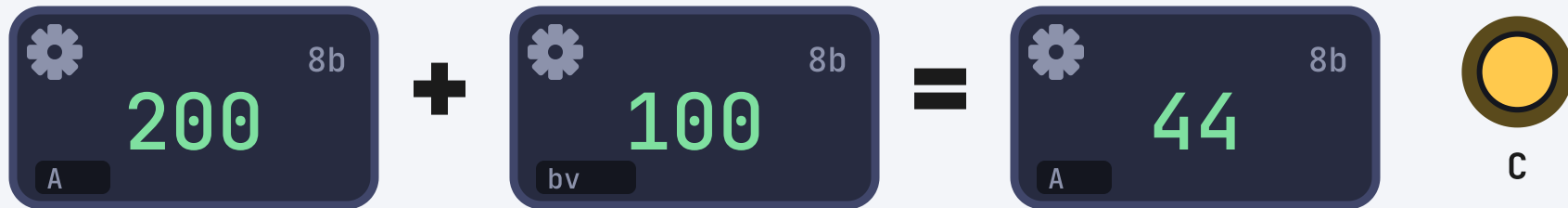




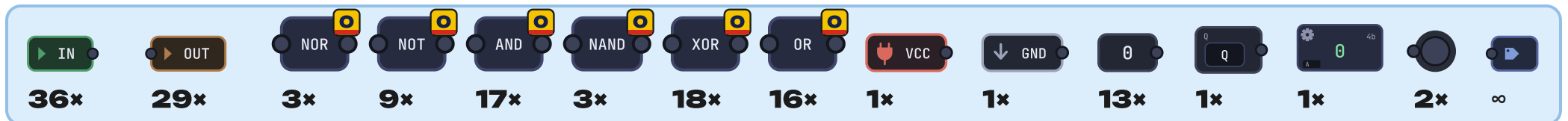
ALU and register A

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a calculator on switches: 9 operations, flags C and Z

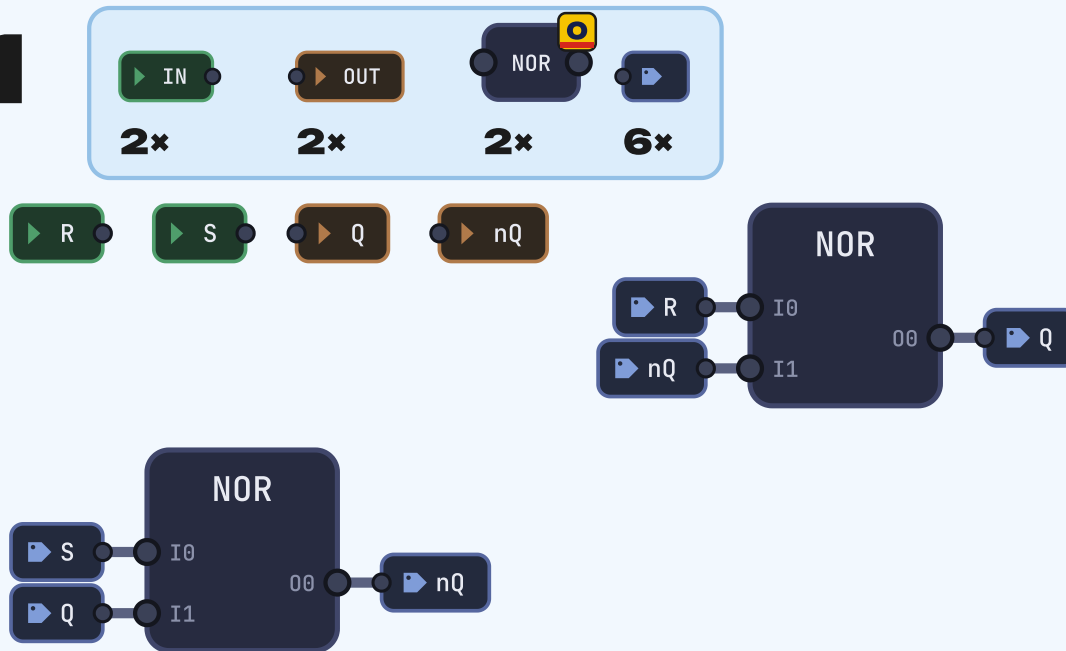


$$200 + 100 = 300 - 256 = 44, C = 1$$

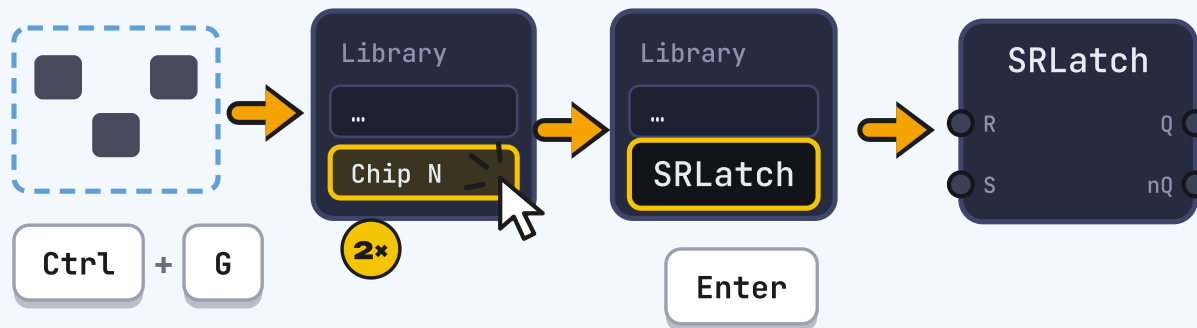


SRLatch

1

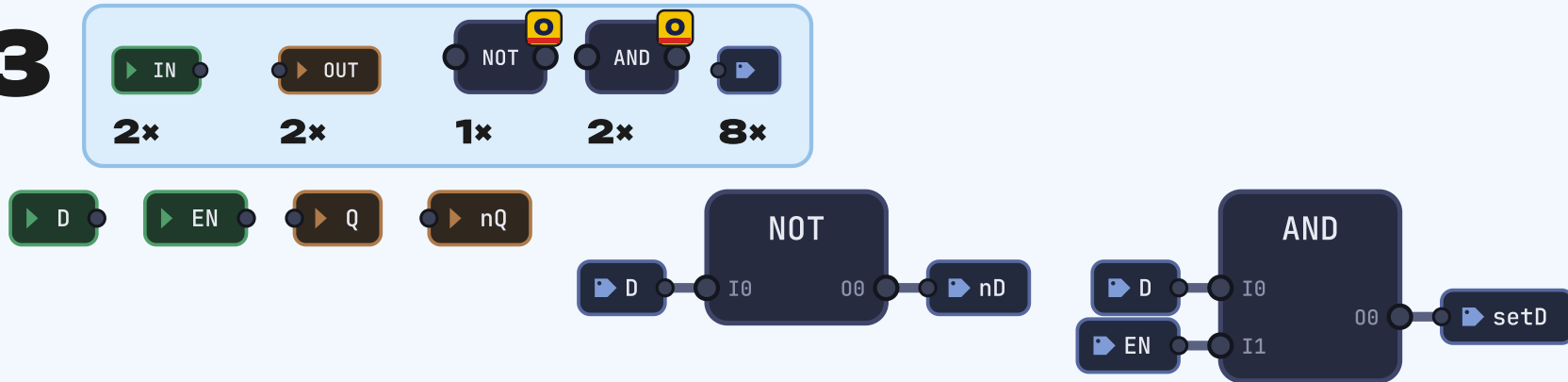


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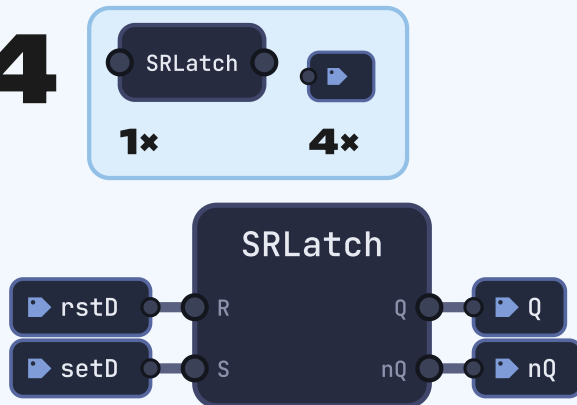


DLatch

3

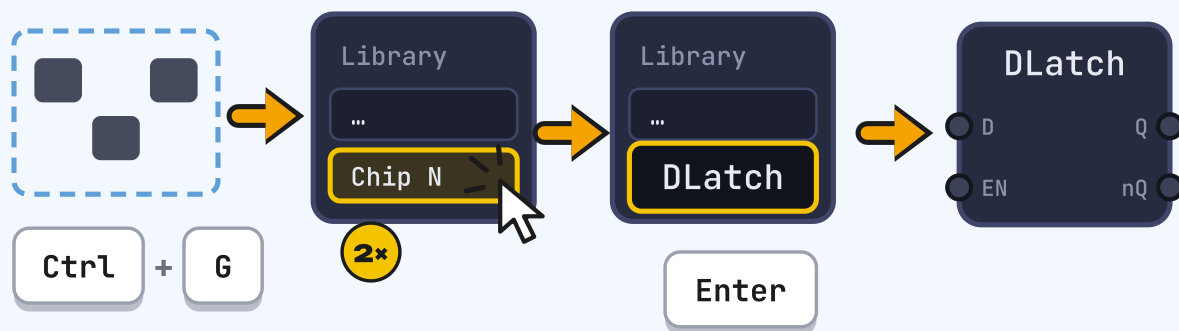


4



DLatch ...

5



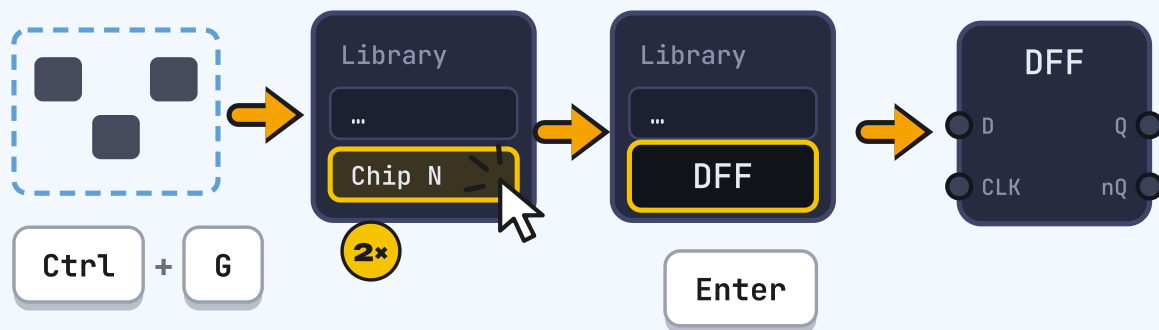
DFF

6



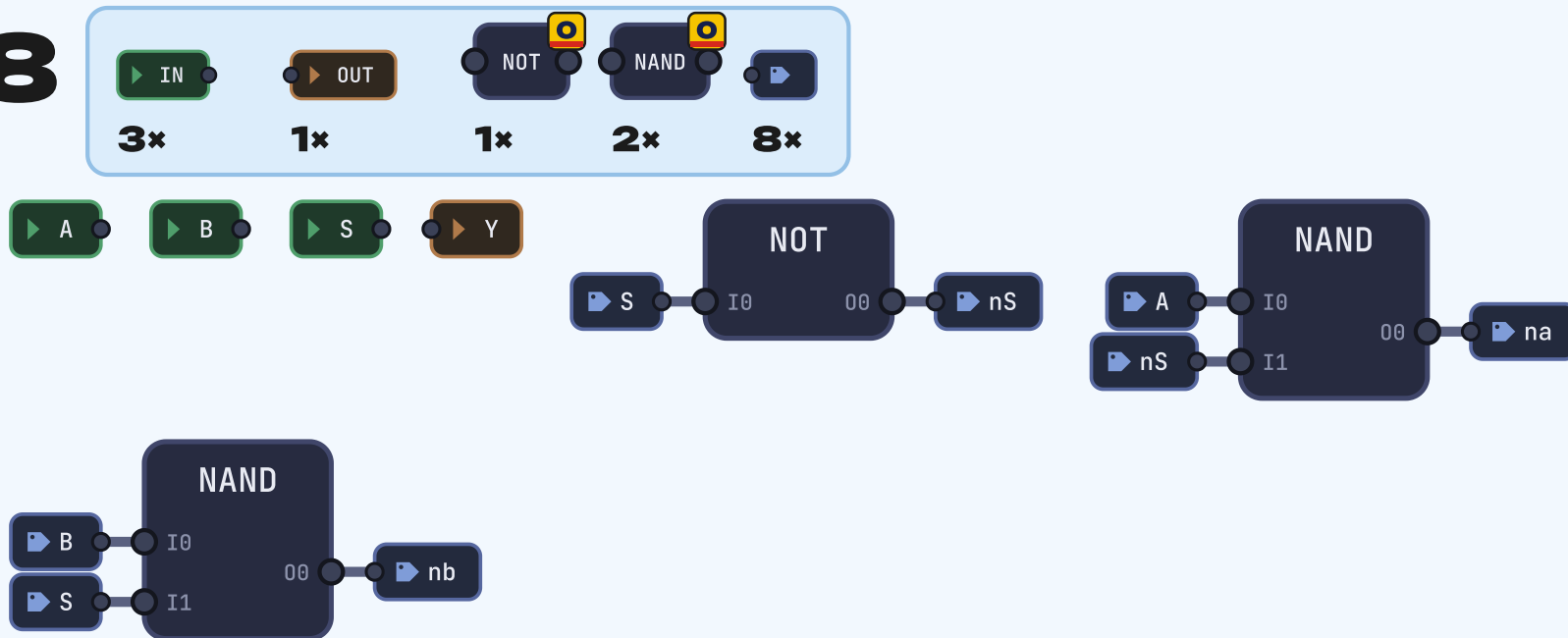
DFF ...

7



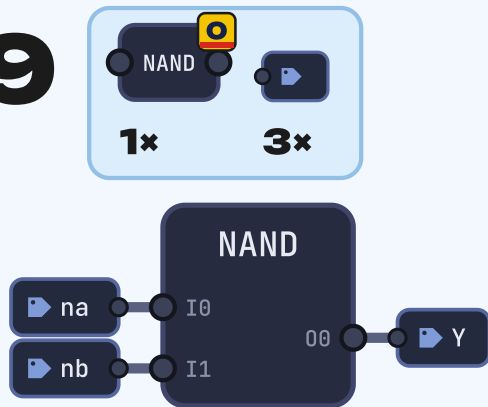
MUX2

8

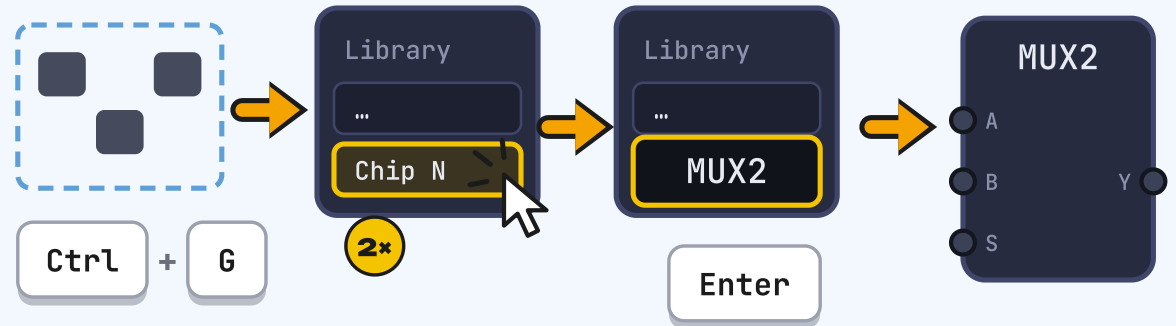


MUX2 ...

9

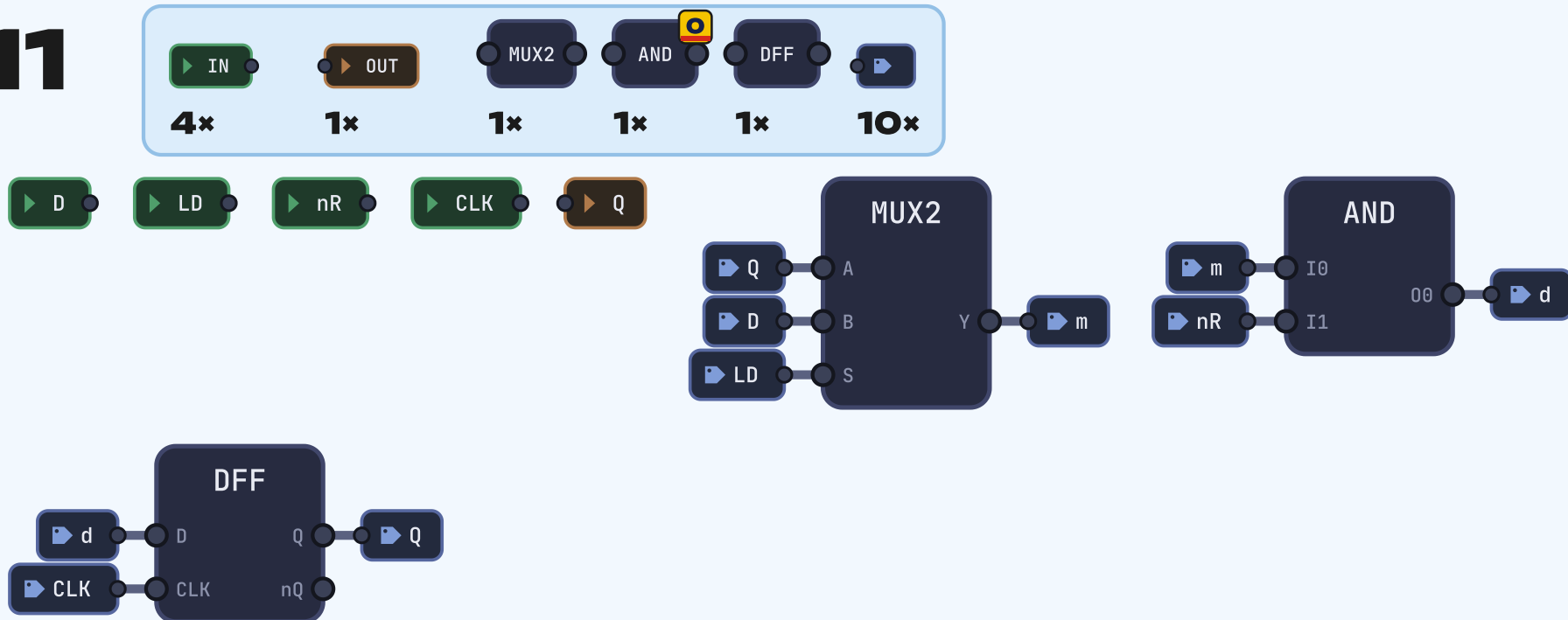


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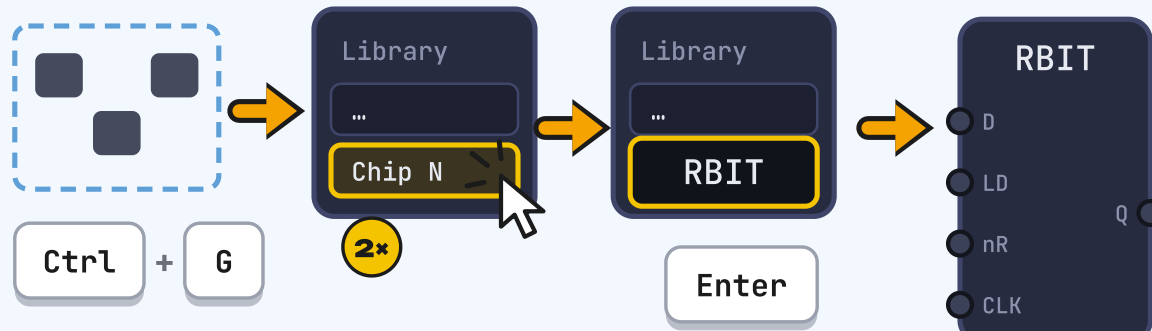
RBIT

11



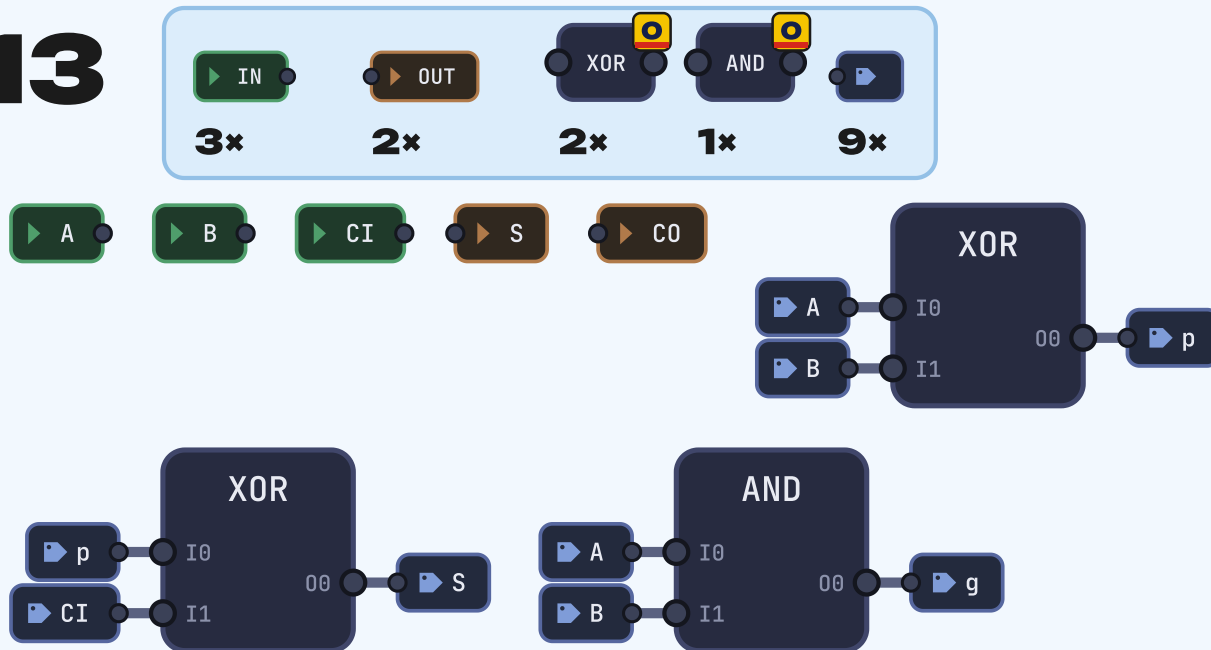
RBIT ...

12



FA

13

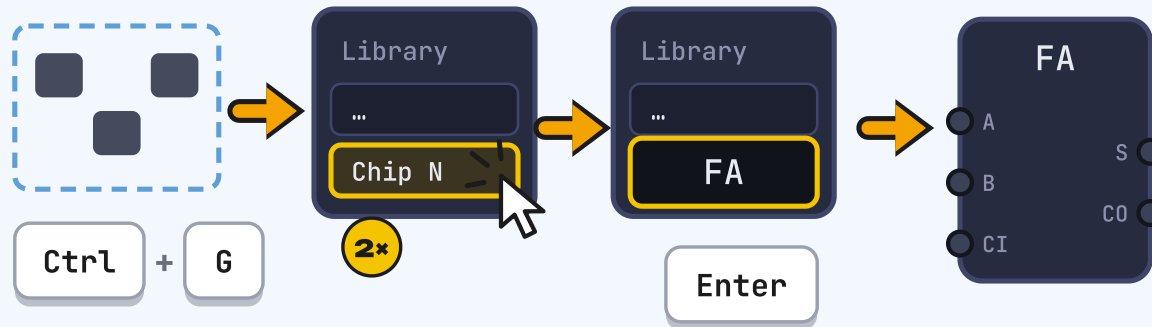


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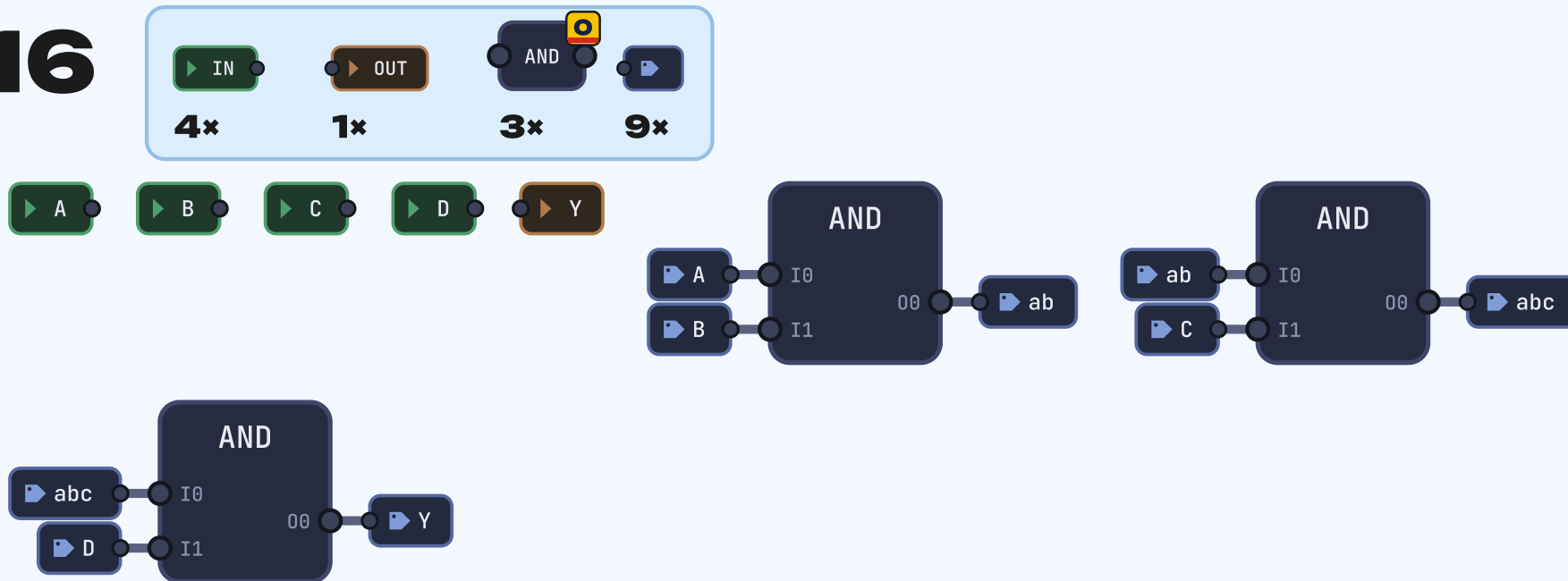
FA...

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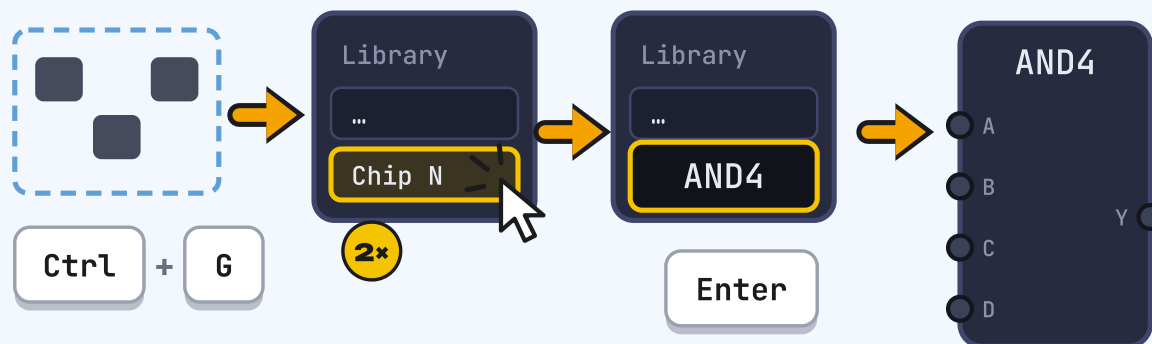
AND4

16



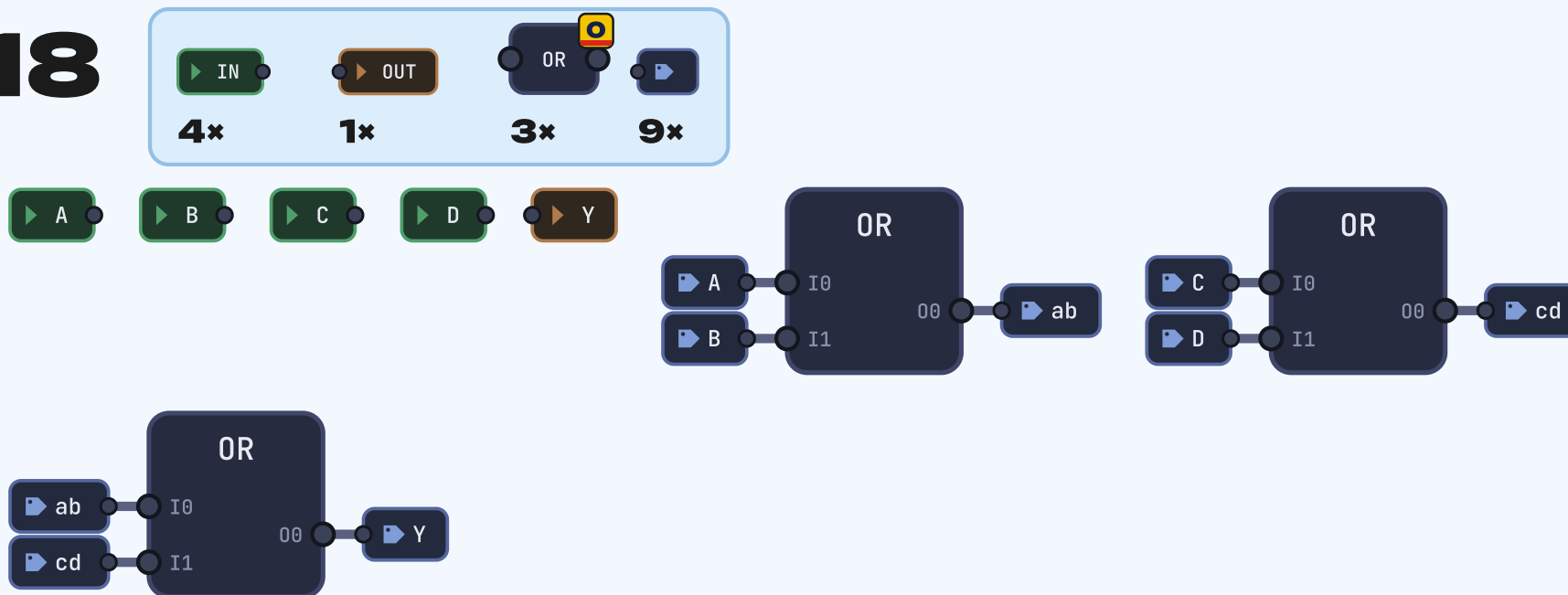
AND4 ...

17



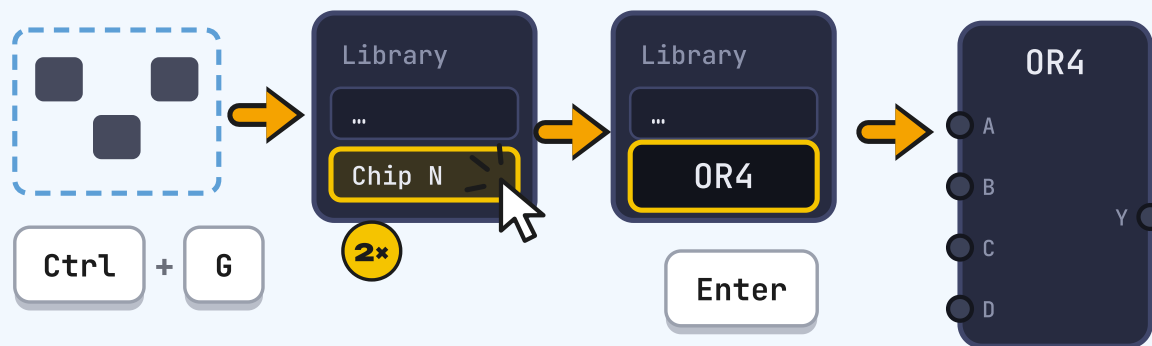
OR4

18



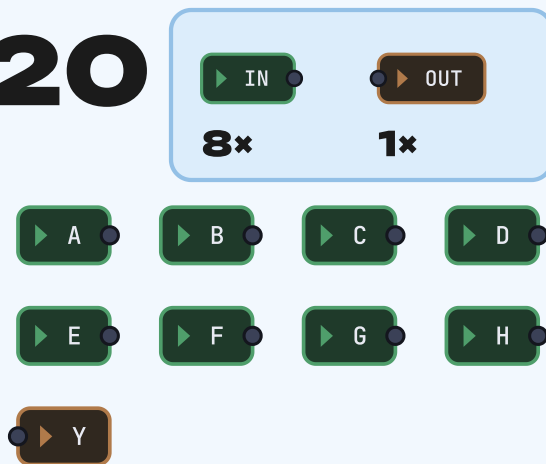
OR4 ...

19

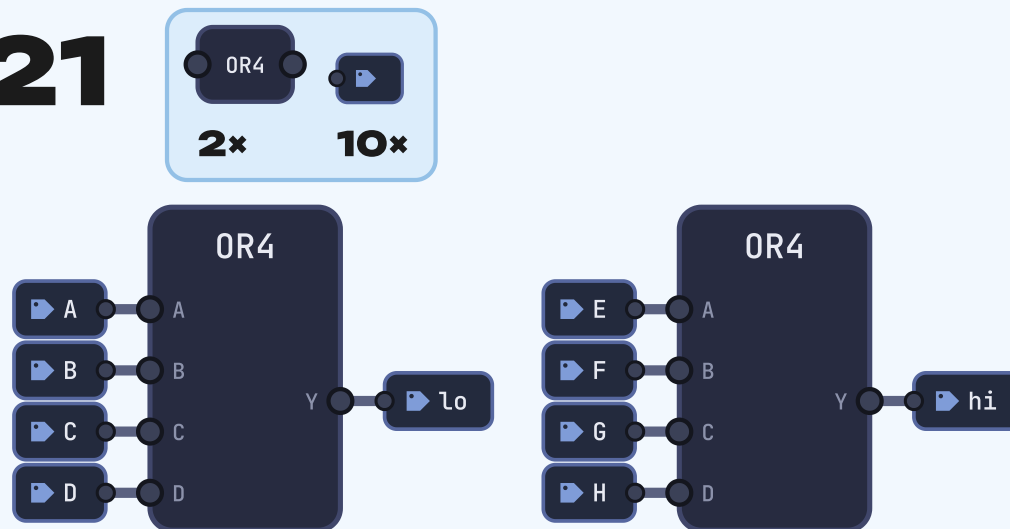


OR8

20

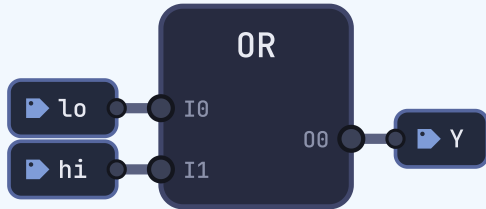
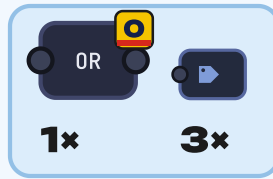


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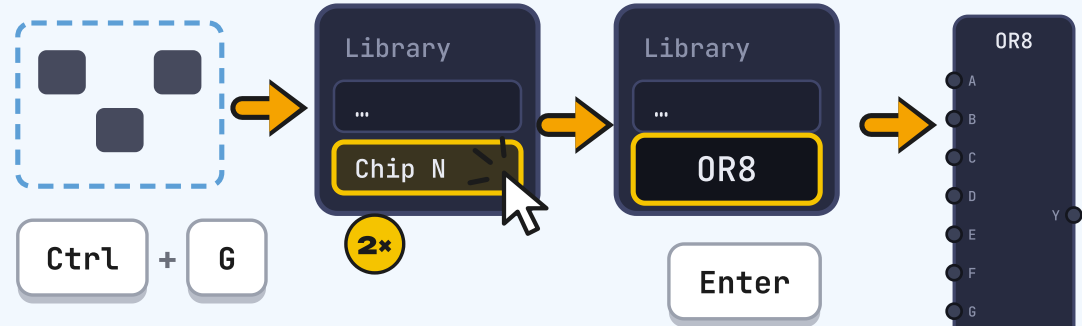


OR8 ...

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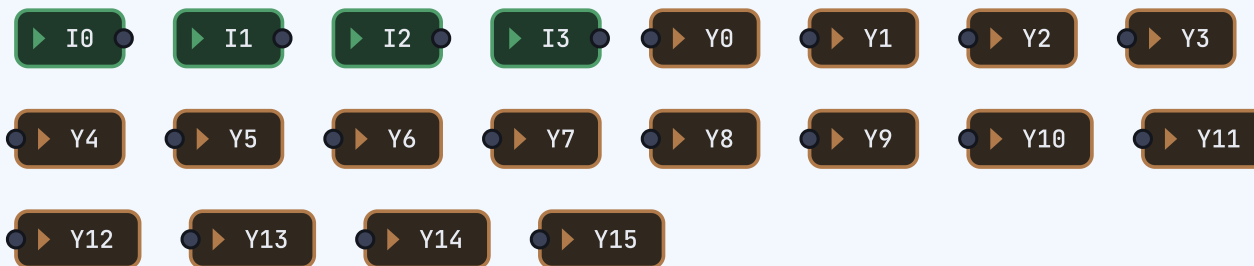
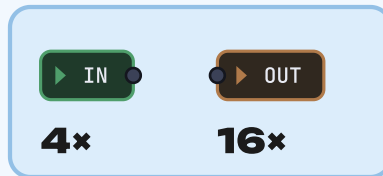


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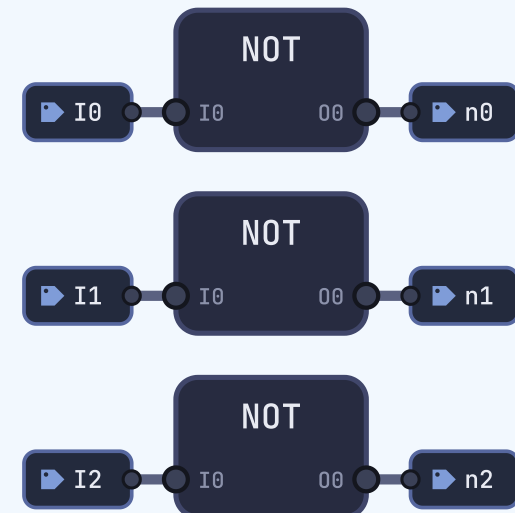
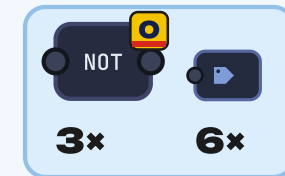


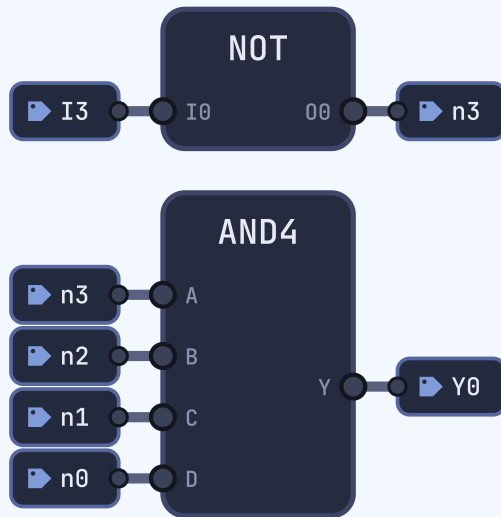
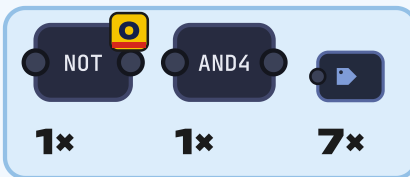
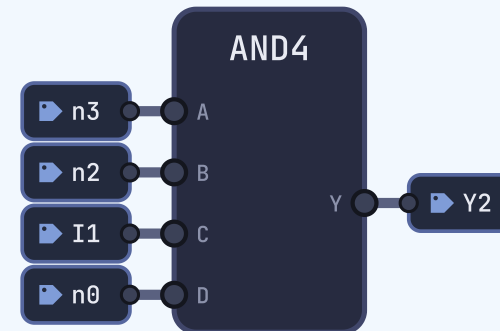
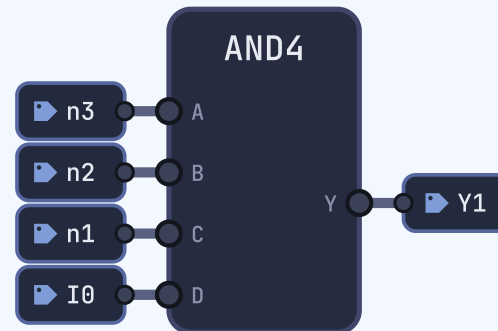
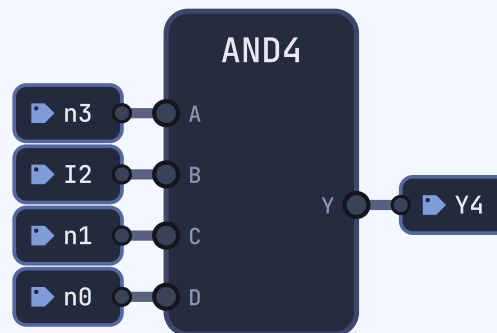
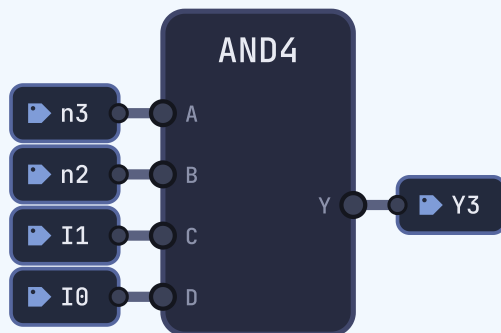
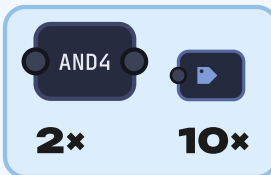
DEC16

24

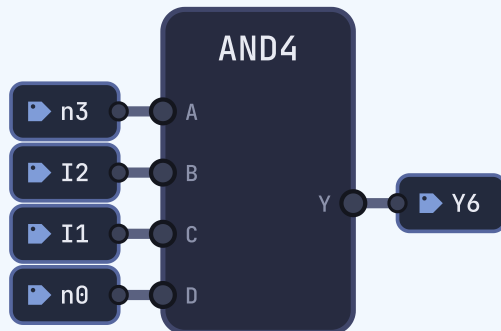
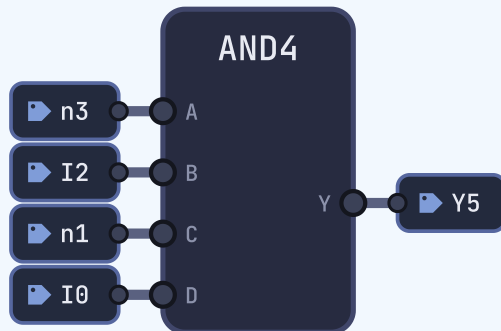


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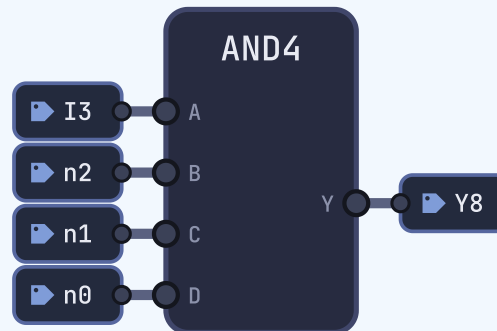
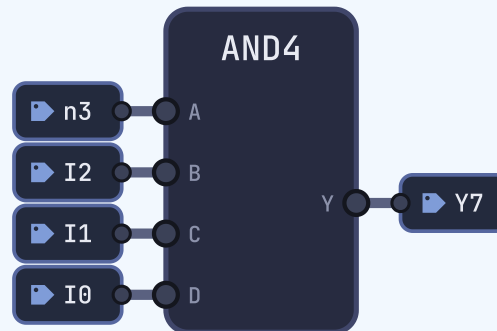


26**27****28**

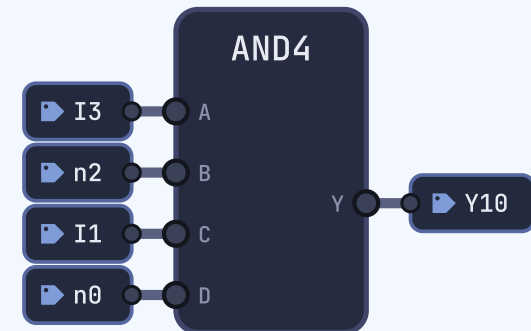
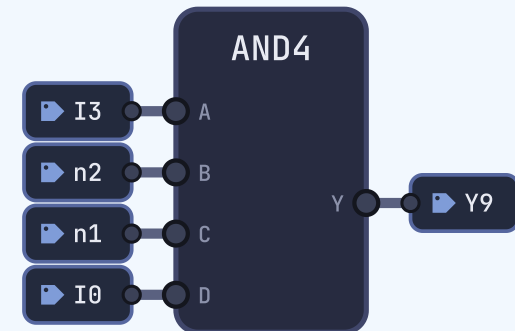
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30



31



DEC16 ...

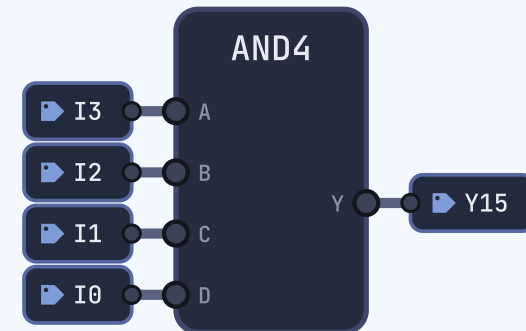
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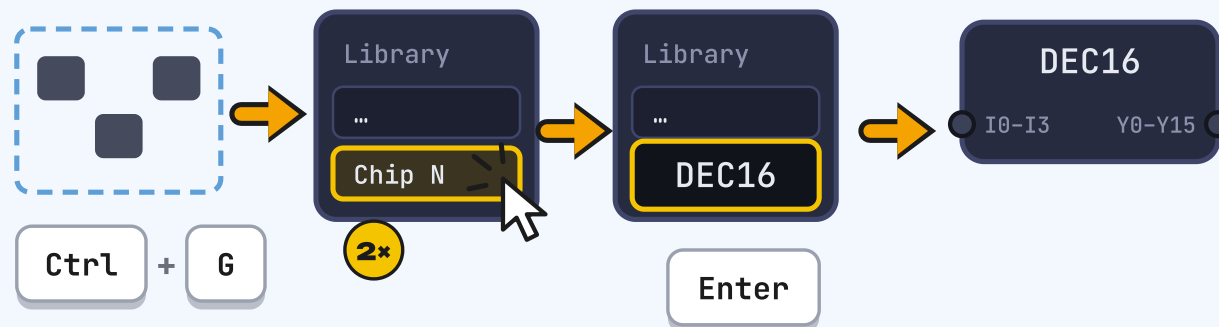
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34



35



36



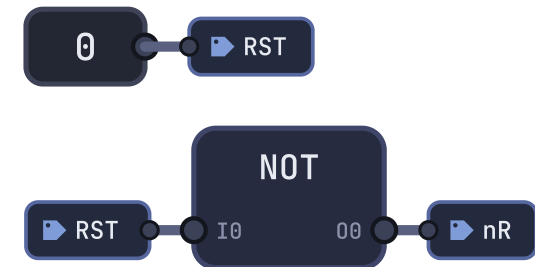
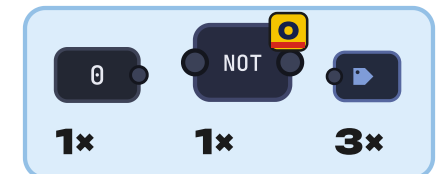
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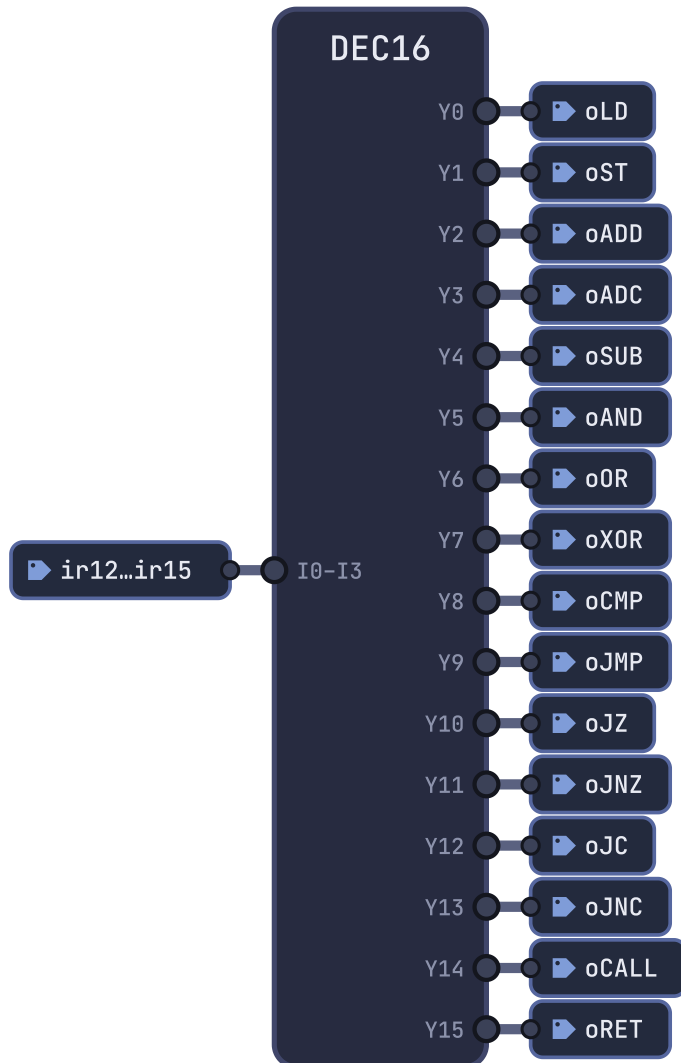
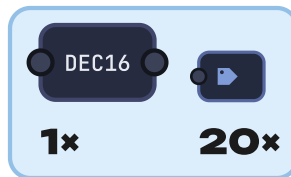
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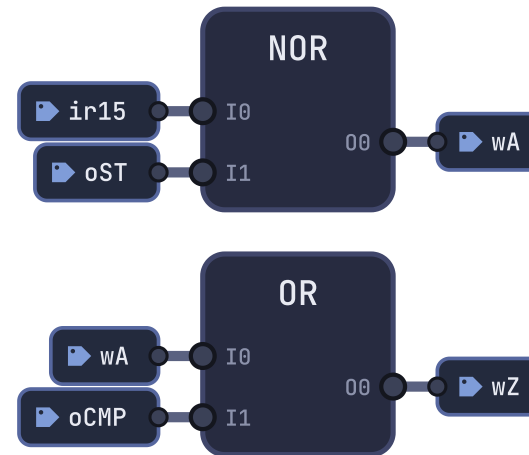
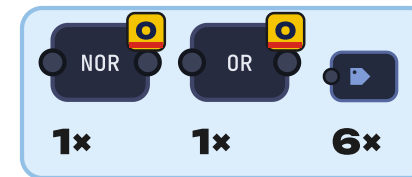
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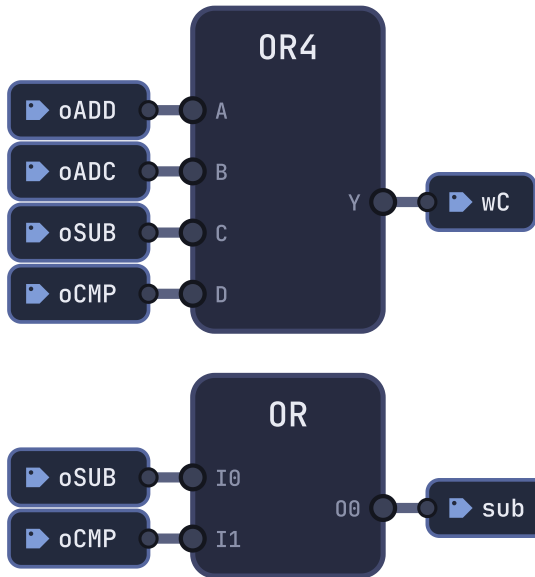
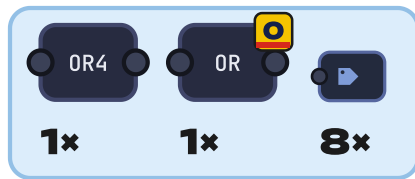
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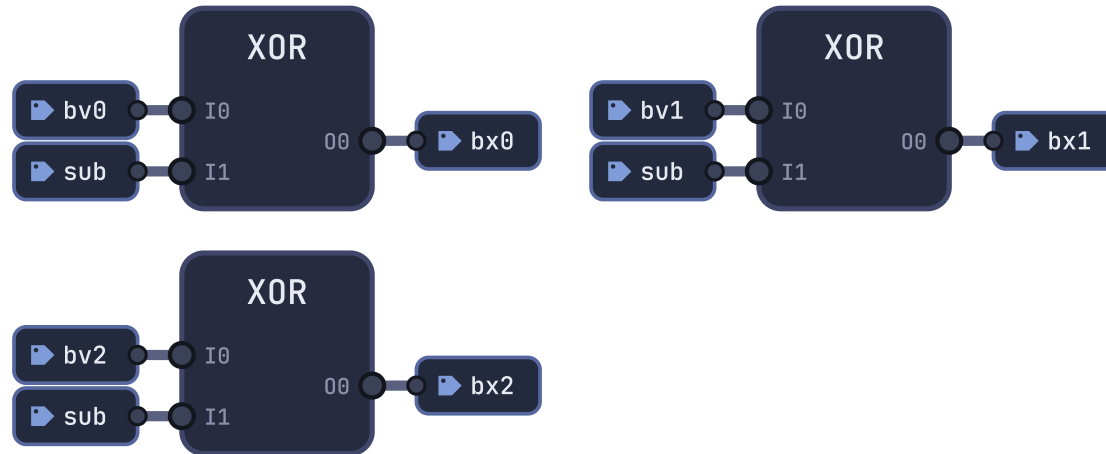
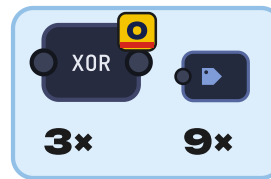
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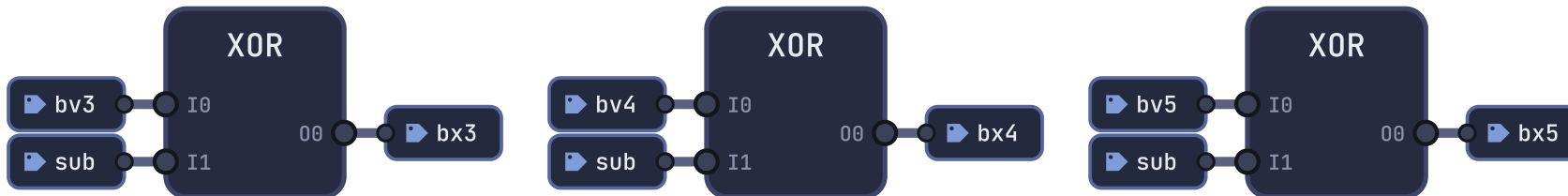
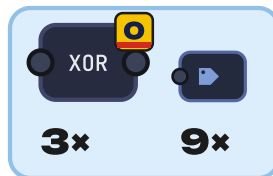
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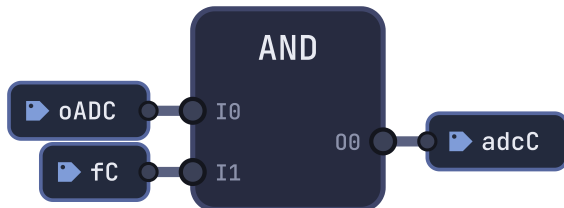
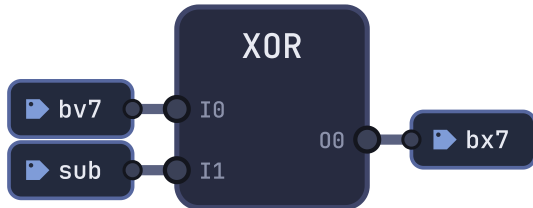
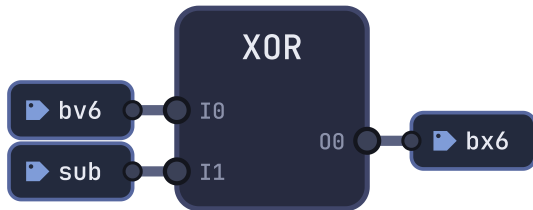
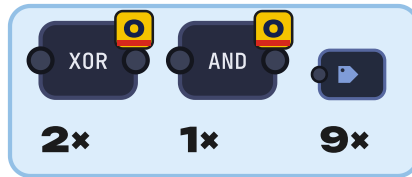
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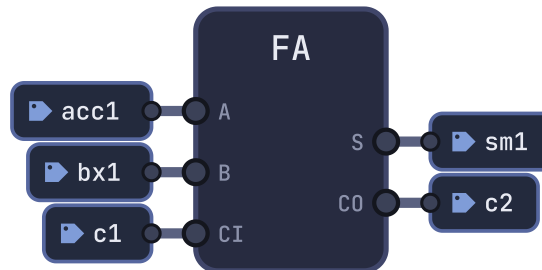
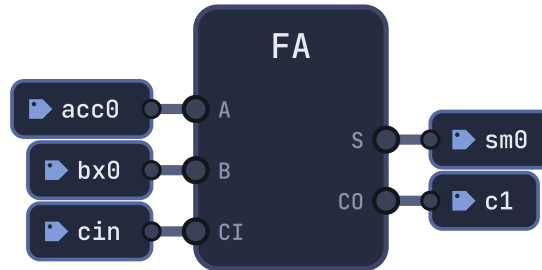
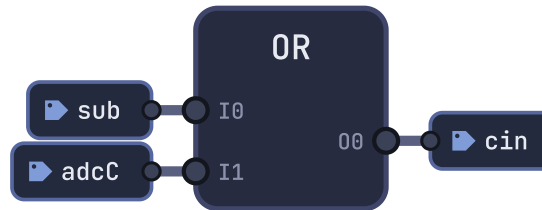
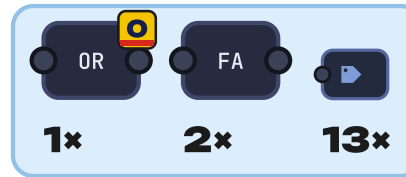
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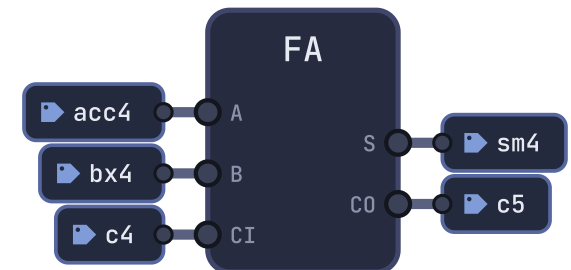
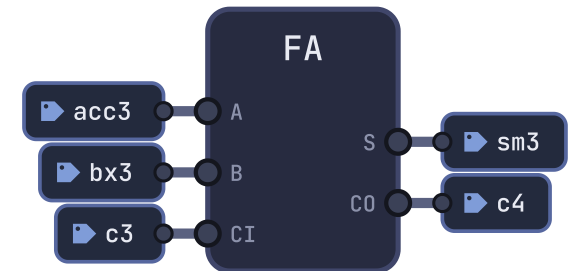
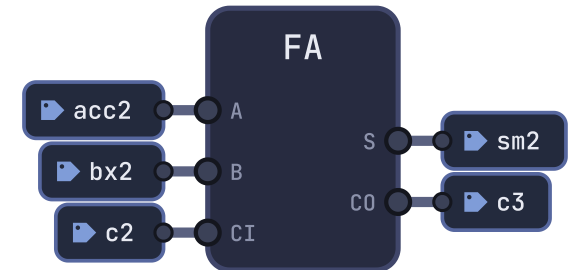
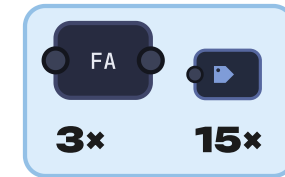
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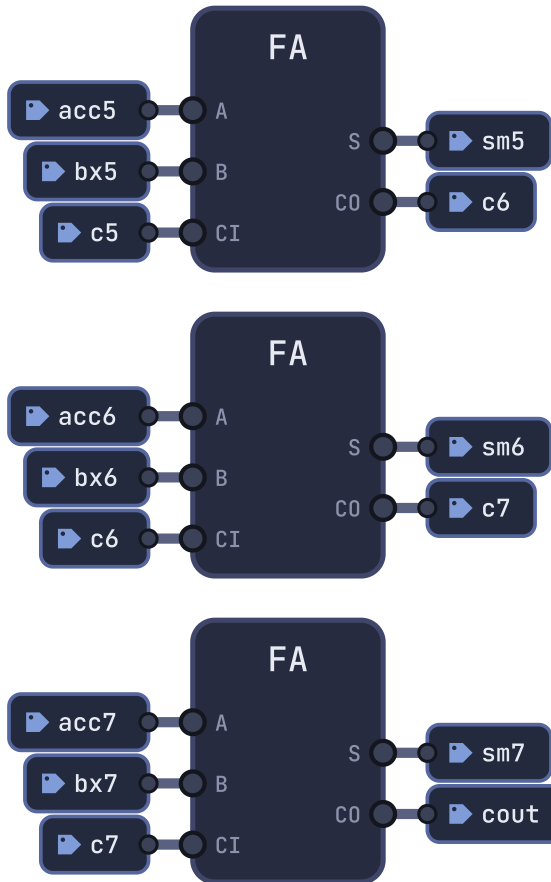
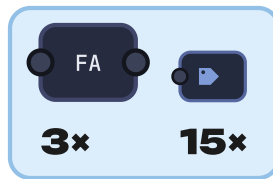
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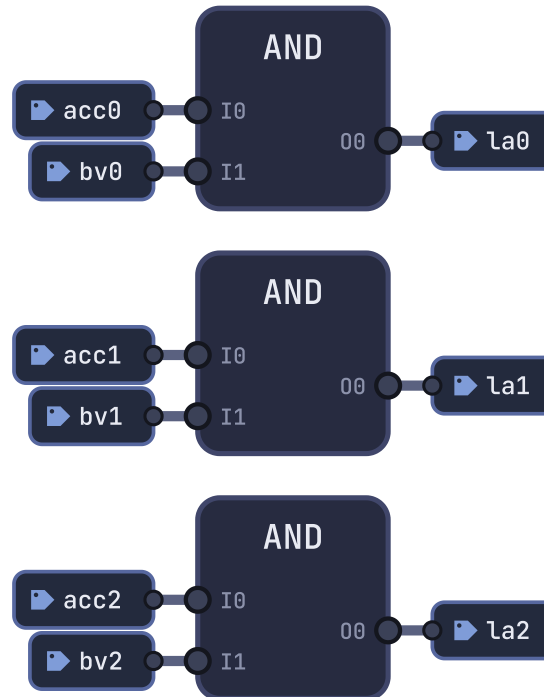
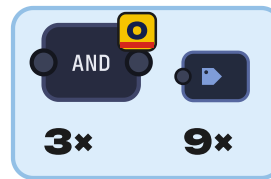
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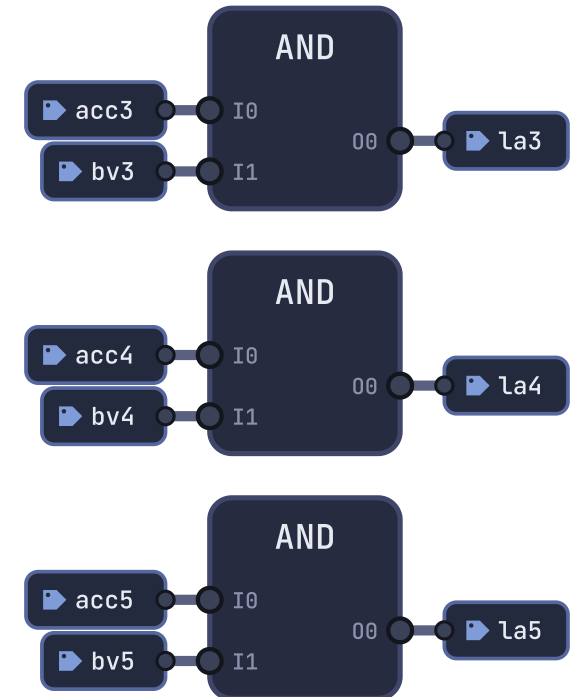
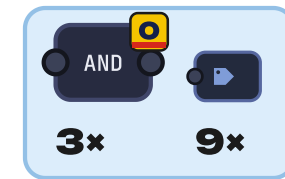
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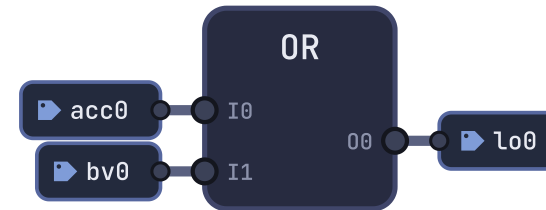
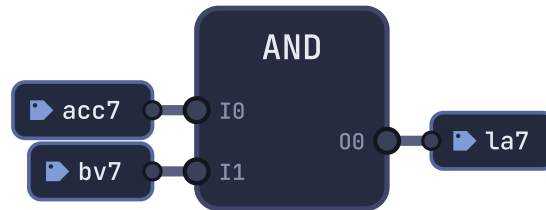
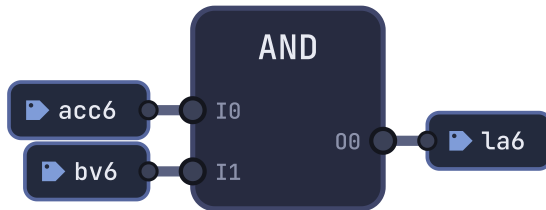
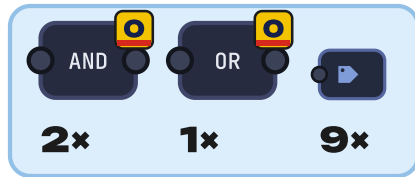
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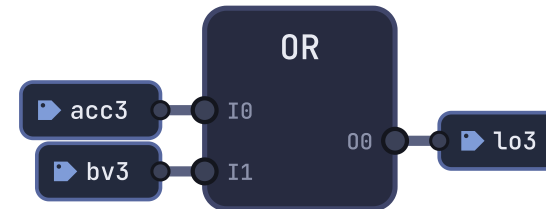
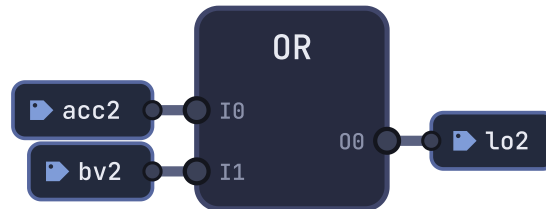
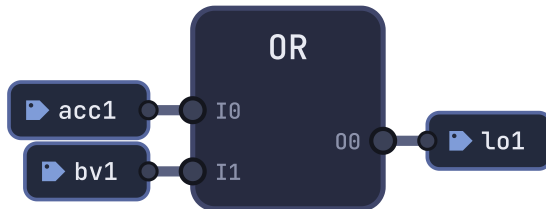
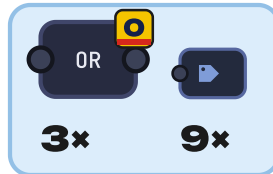
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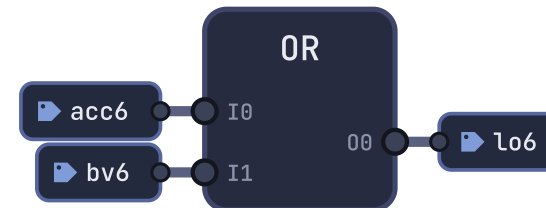
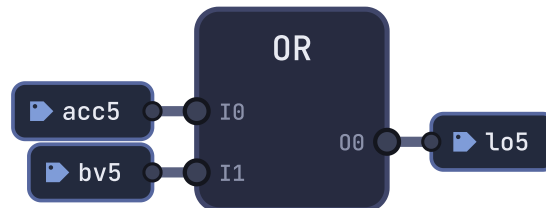
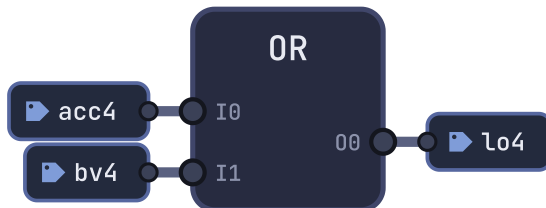
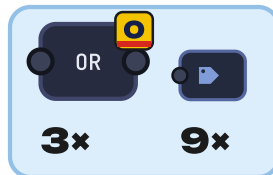
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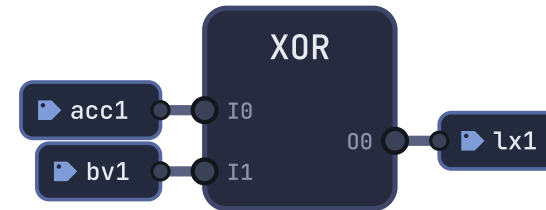
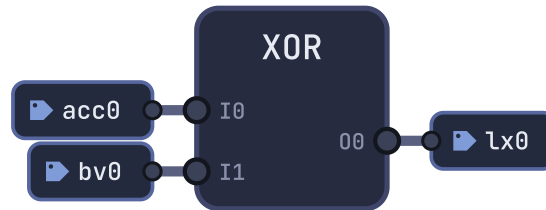
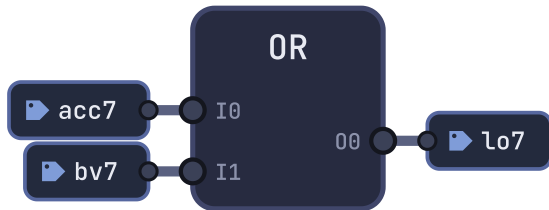
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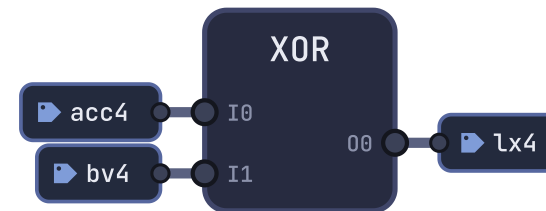
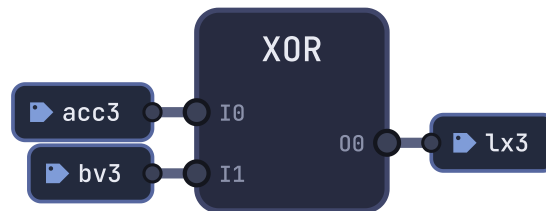
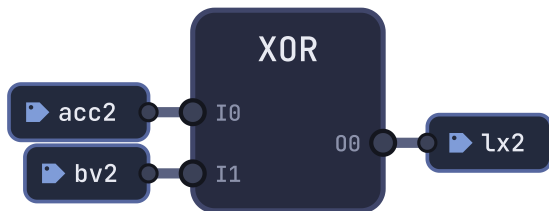
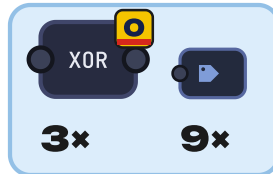
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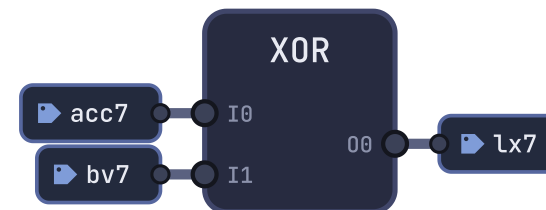
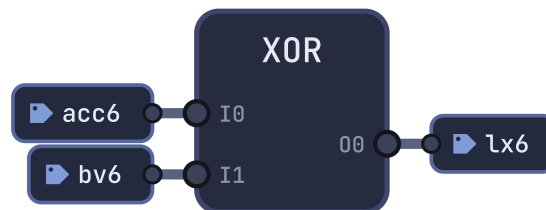
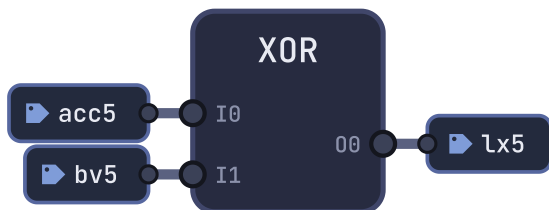
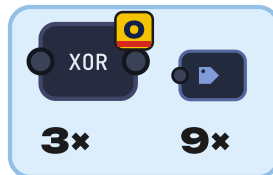
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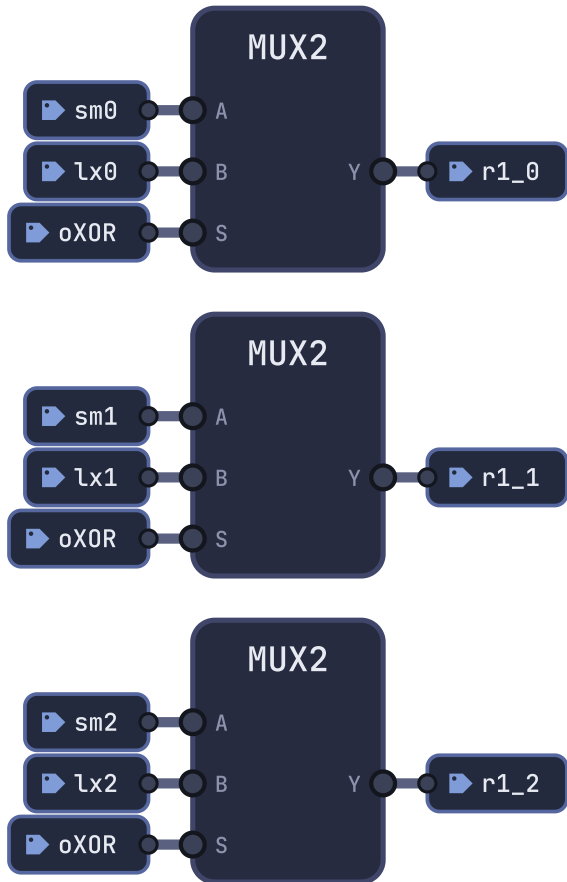
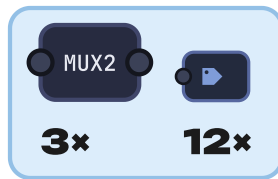
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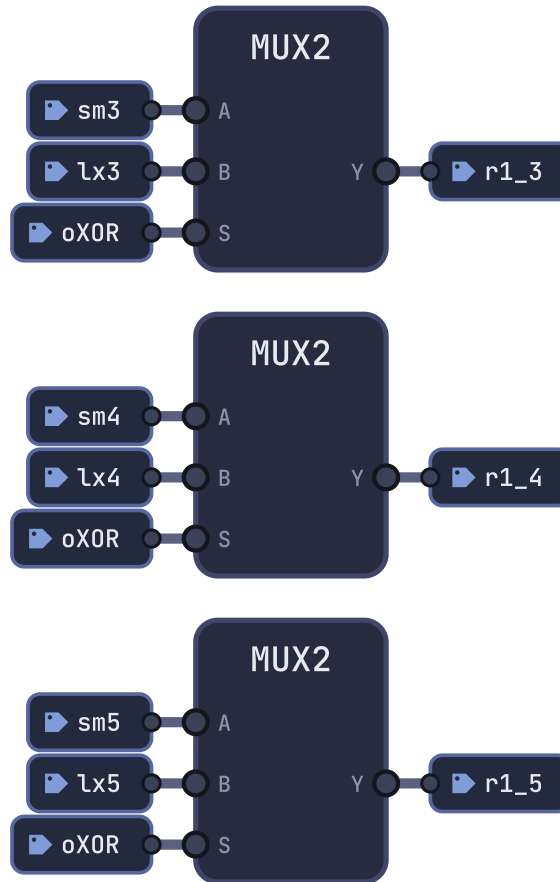
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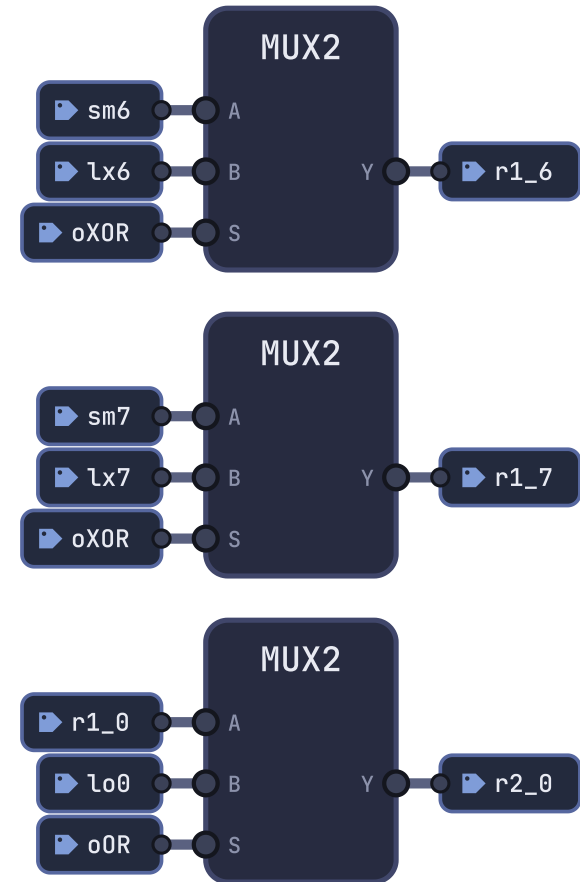
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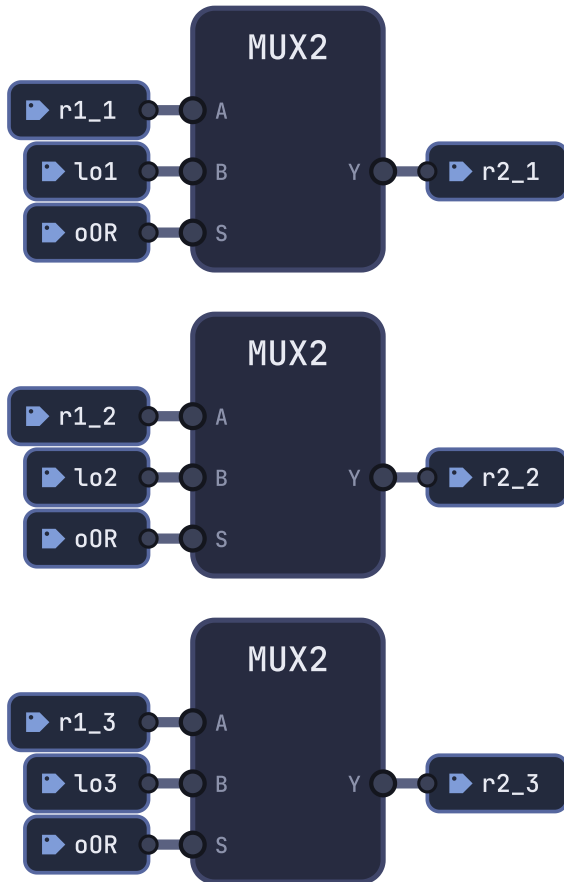
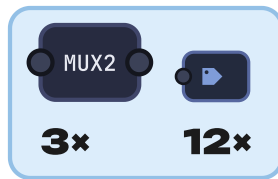
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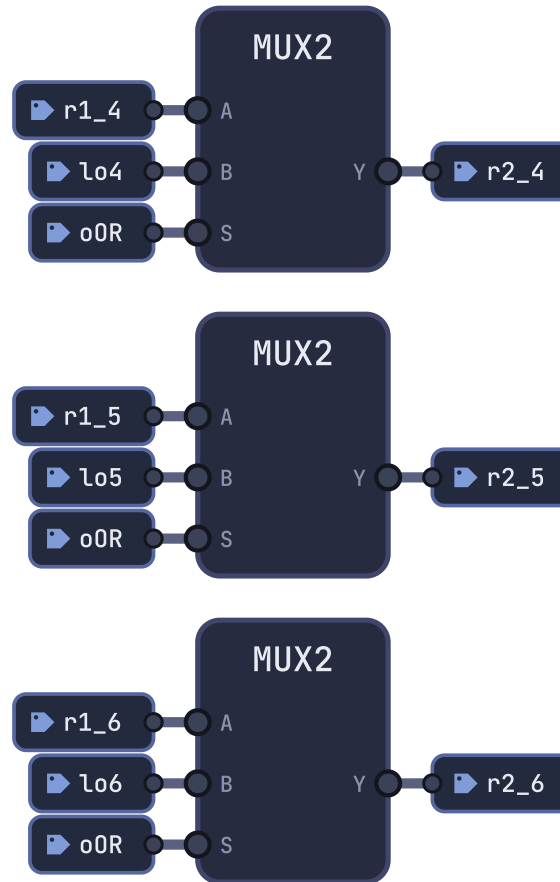
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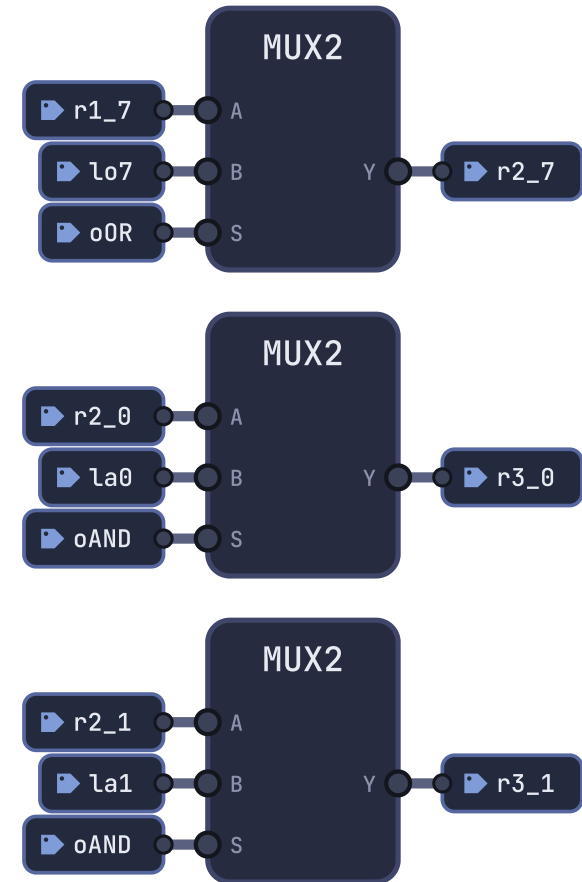
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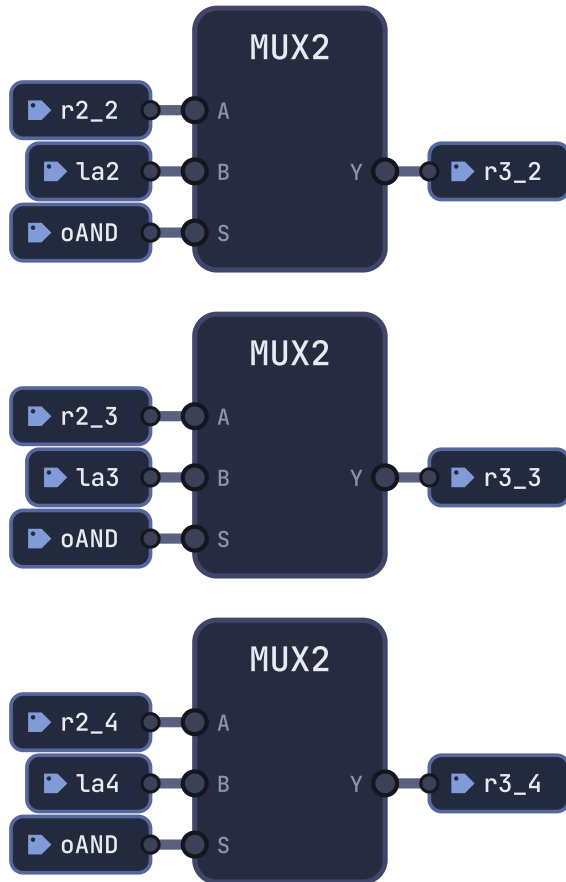
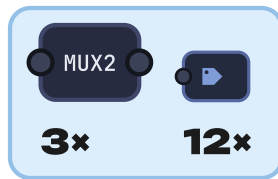
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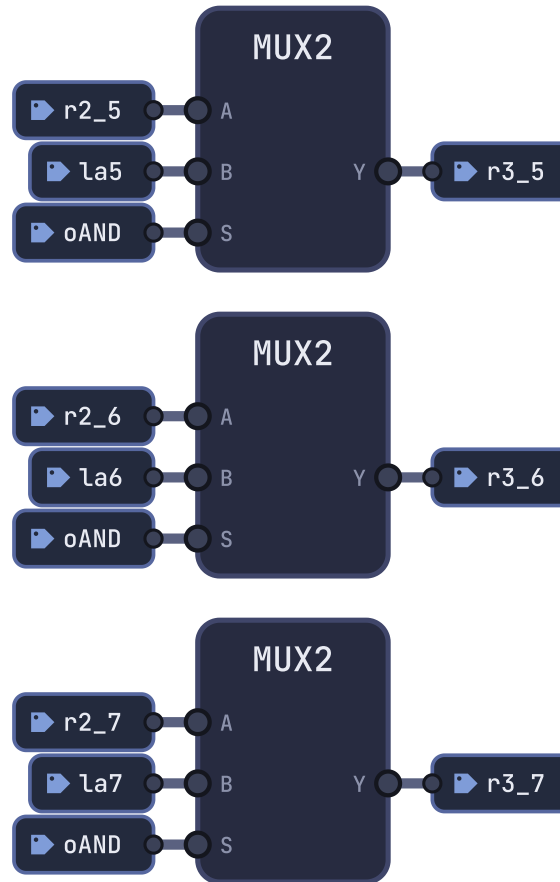
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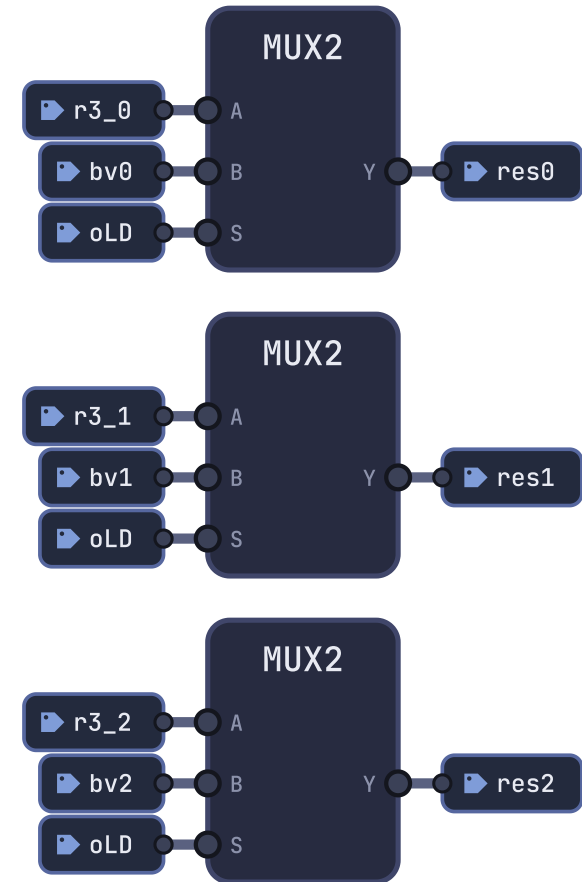
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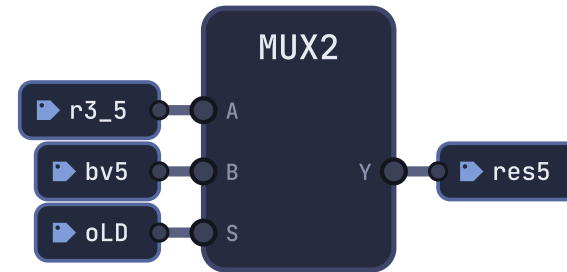
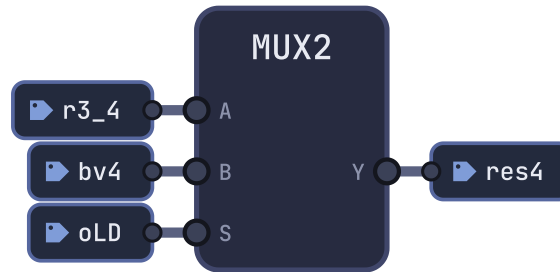
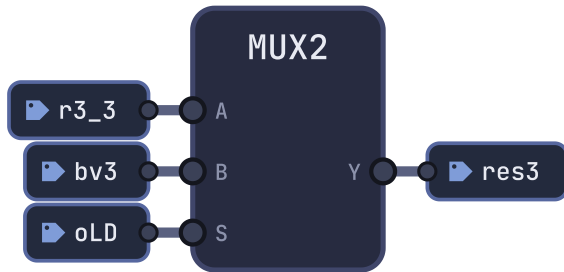
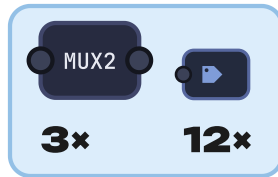
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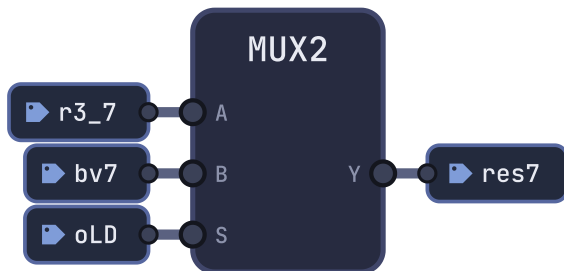
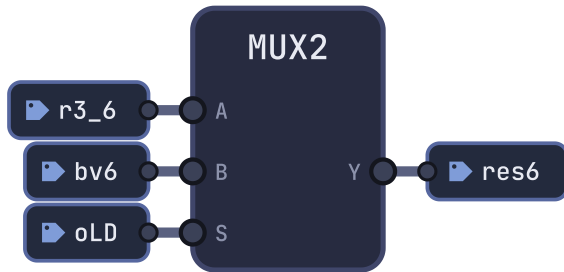
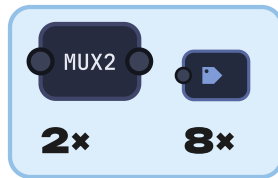
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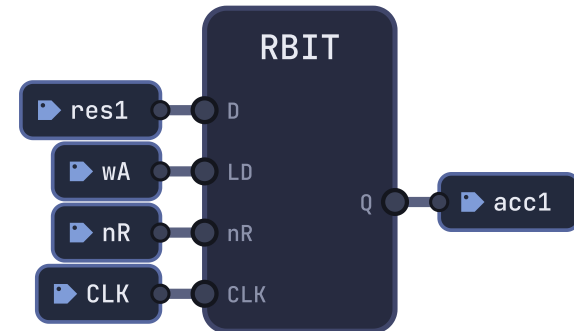
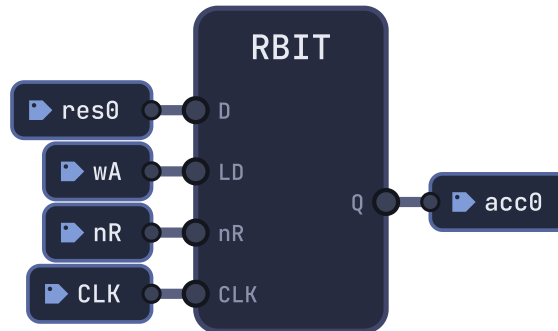
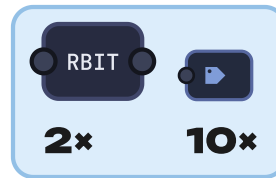
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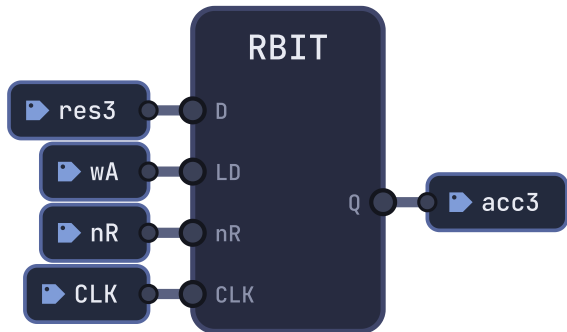
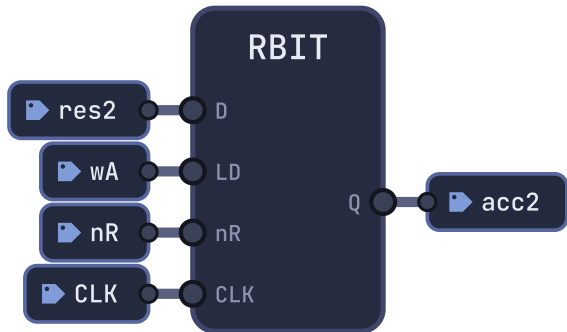
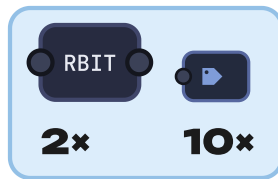
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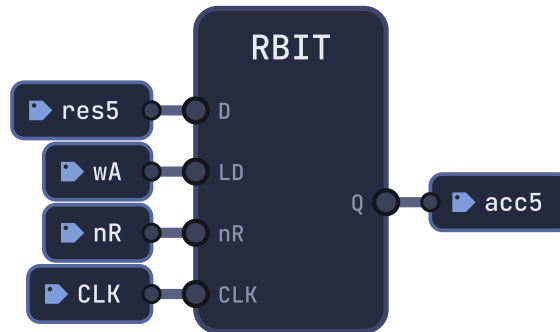
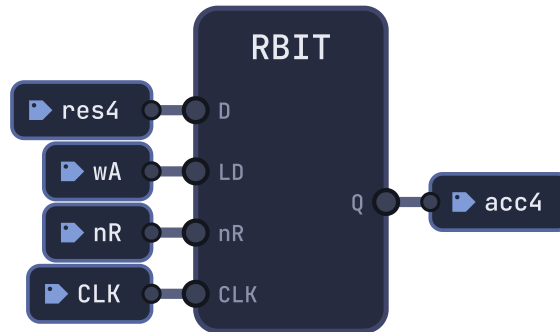
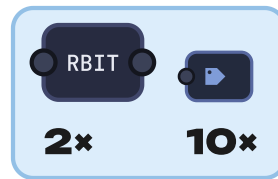
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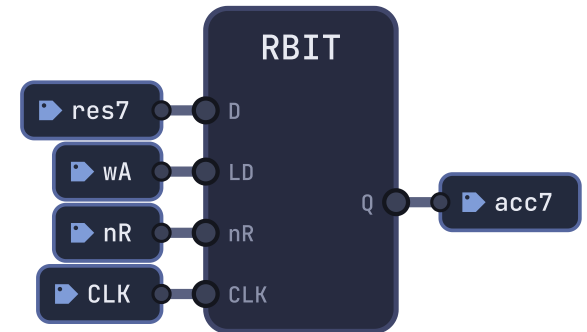
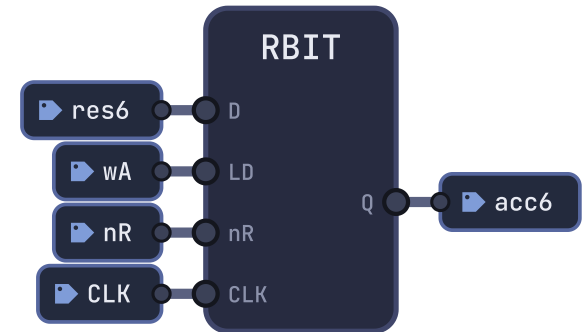
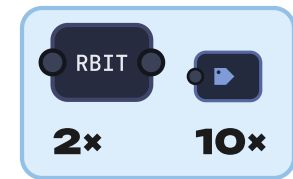
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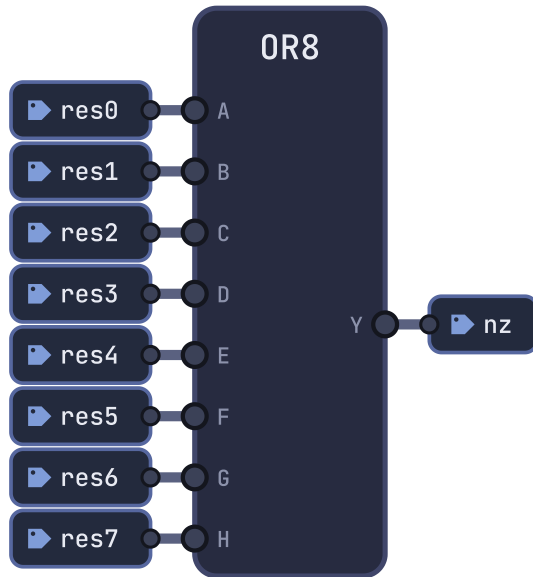
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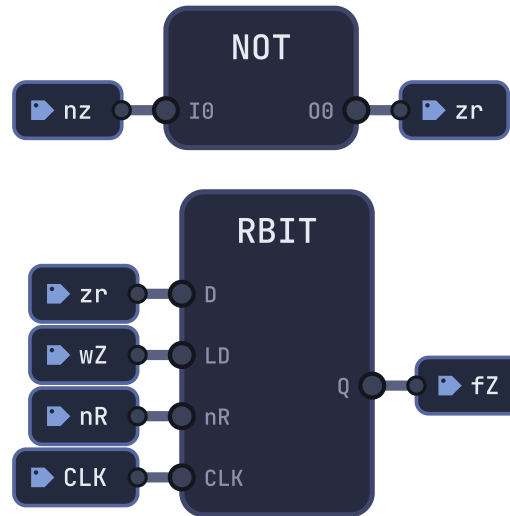
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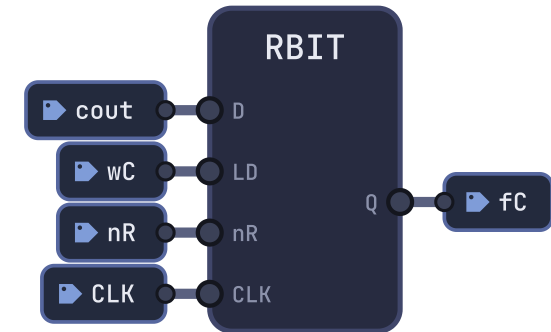
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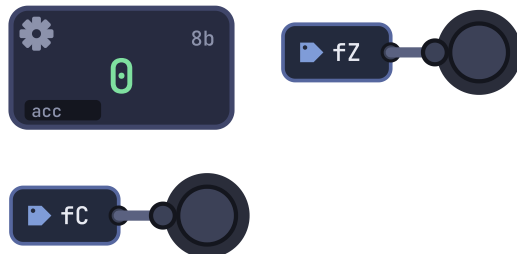
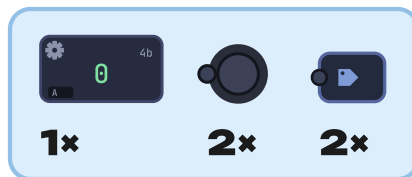
73



74



75



LD

0000 1100 1000 (200)

ADD

0010 0110 0100 (100)

SUB

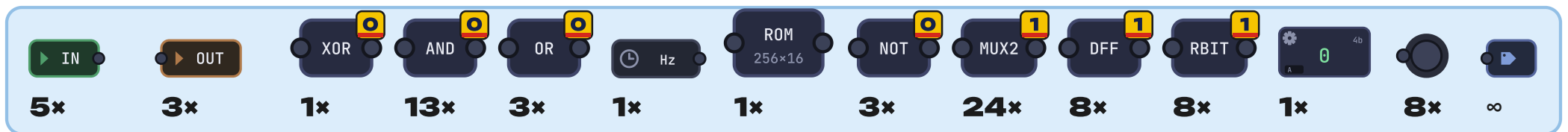
0100 0010 1100 (44)





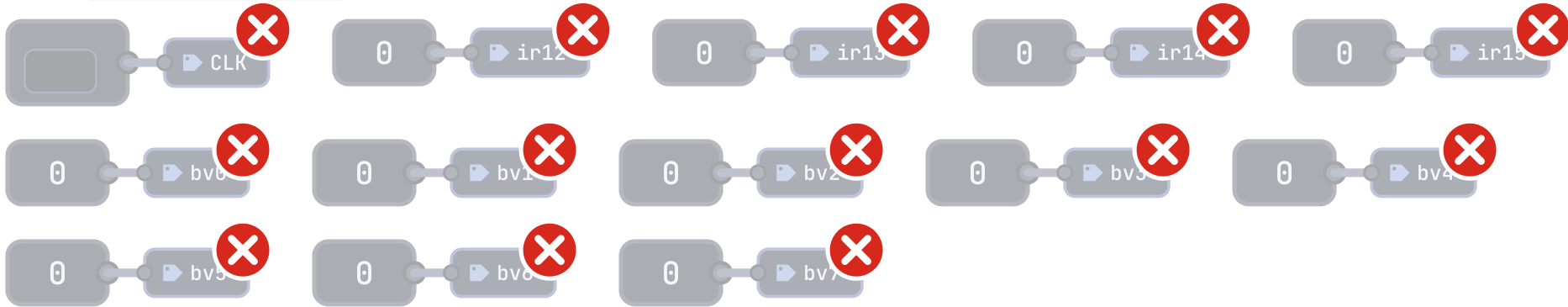
Program counter and ROM

the processor walks through the program by itself



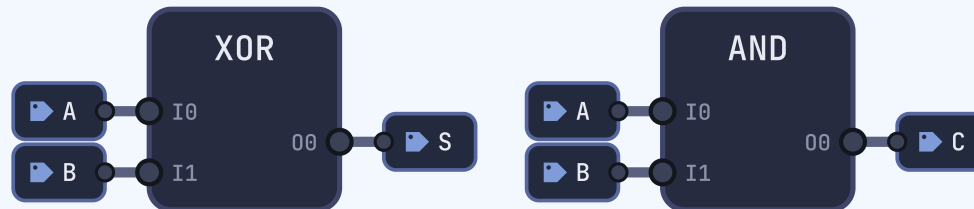
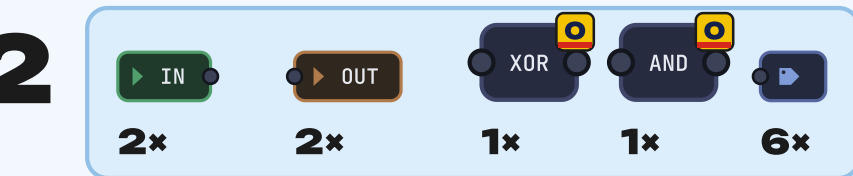
CANVAS

1



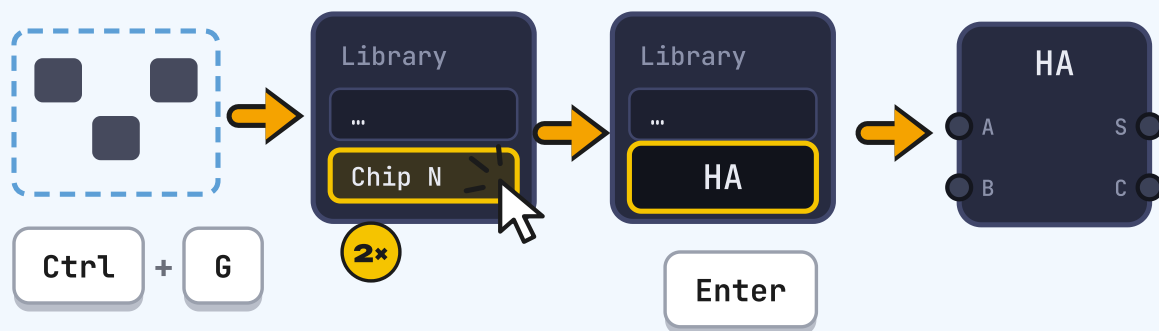
HA

2



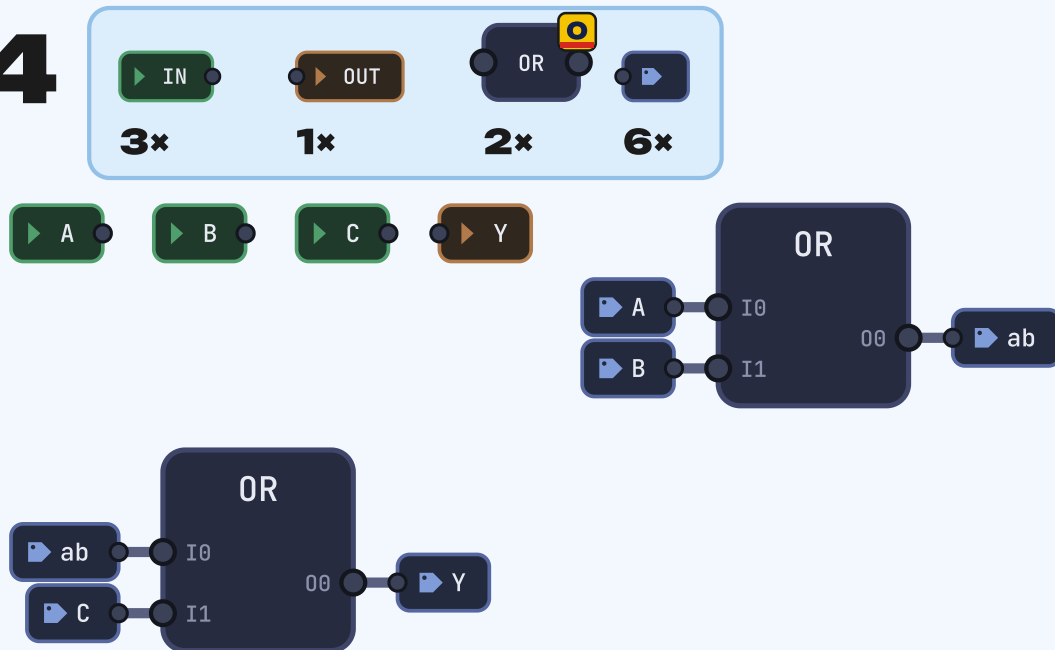
HA ...

3



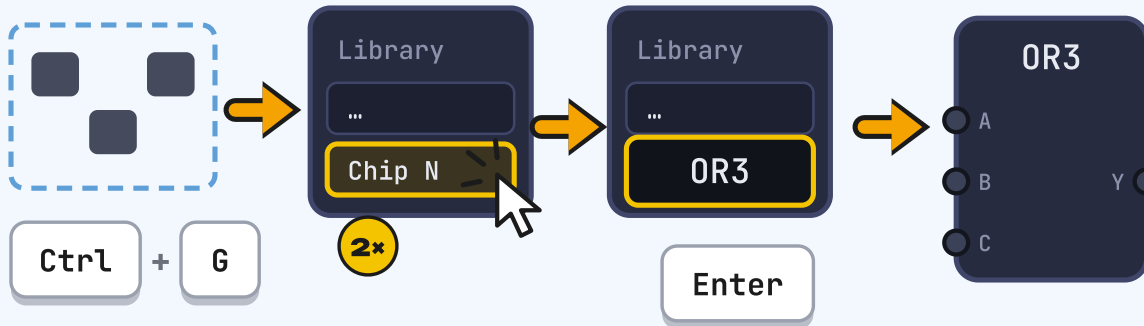
OR3

4



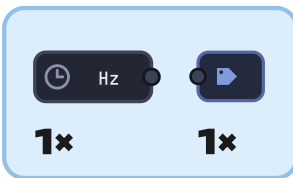
OR3 ...

5



CANVAS

6



7

Memory (RAM) → ⚙: 256 words · 16b data · 16b addr · CLR off

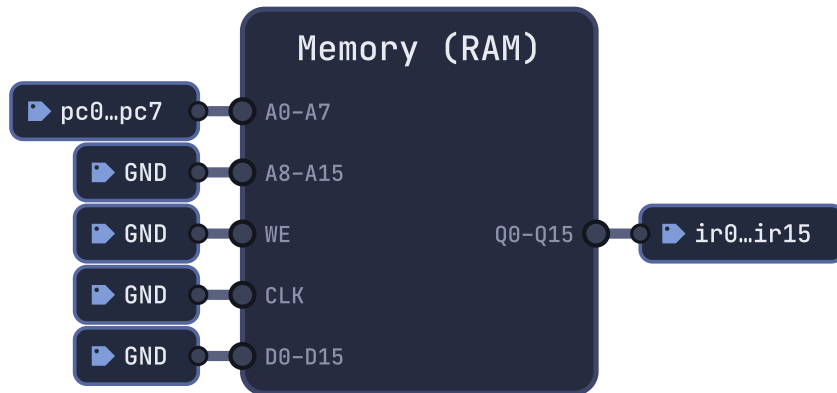
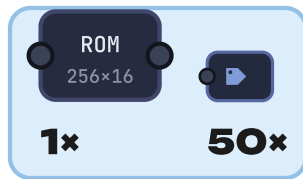
8

legs A8-A15, WE, CLK, D0-D15 – to GND: nobody writes to a ROM

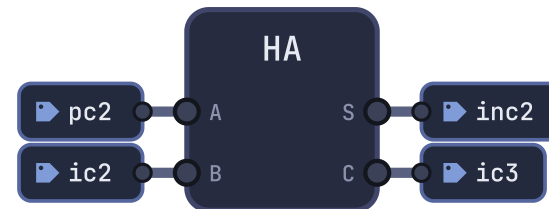
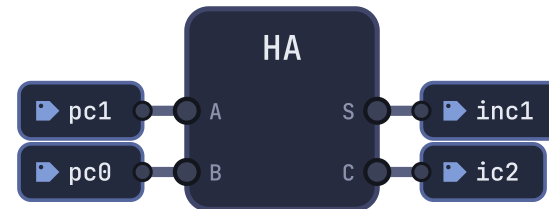
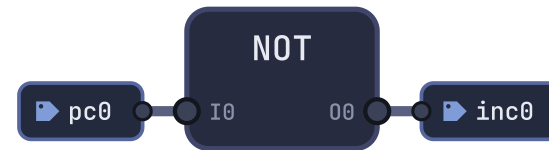
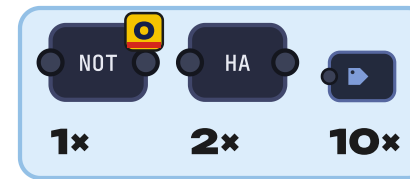
9

pins in a row – one line: A0-A7 → pc0...pc7 means A0 → pc0, A1 → pc1 ... A7 → pc7

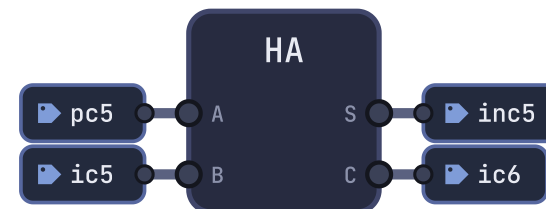
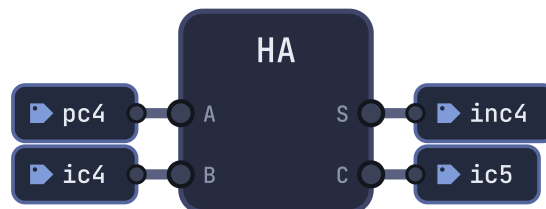
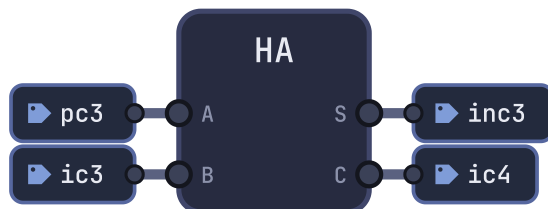
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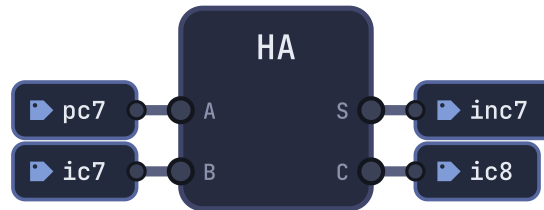
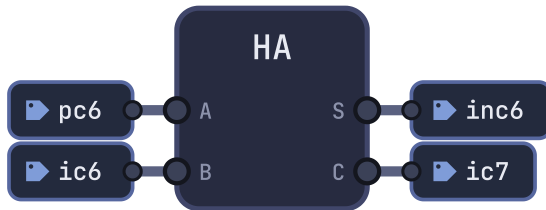
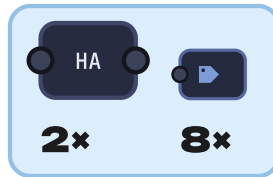
11



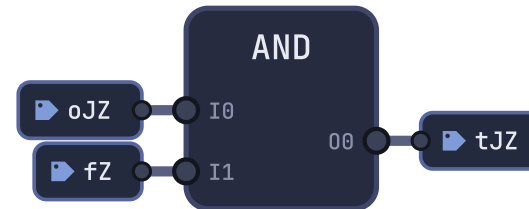
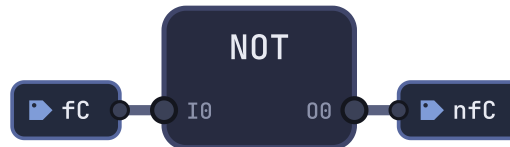
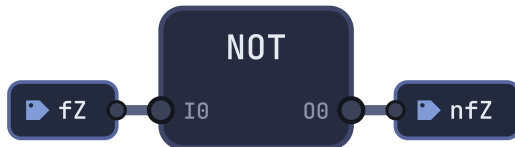
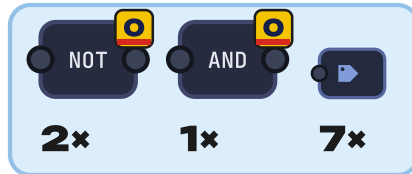
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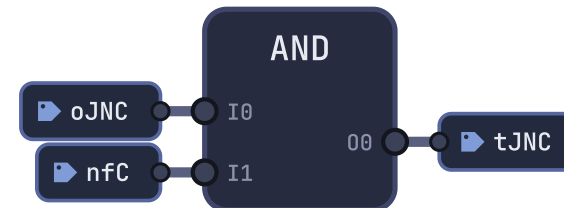
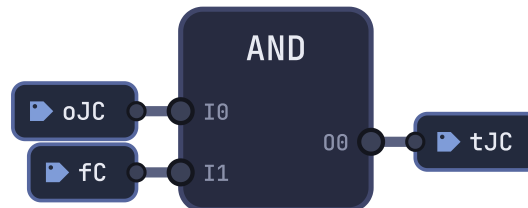
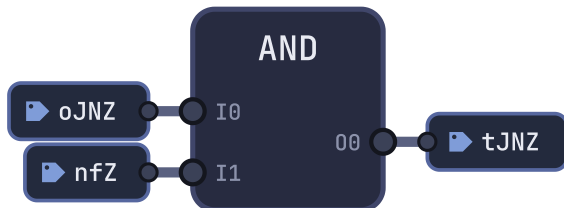
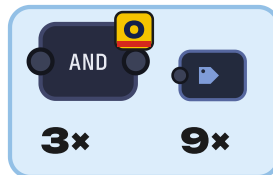
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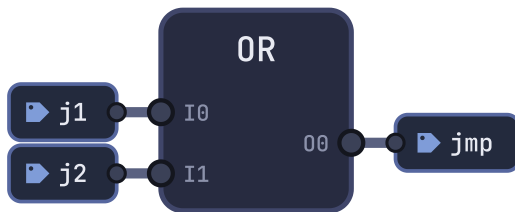
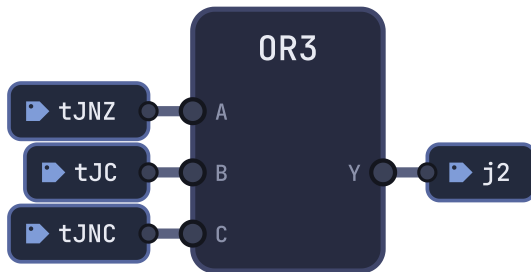
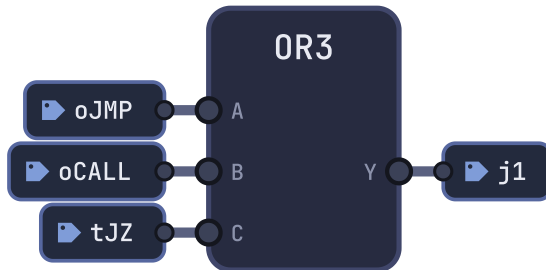
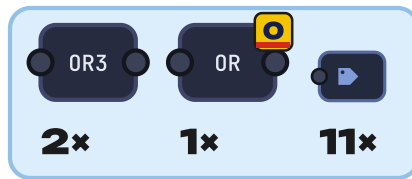
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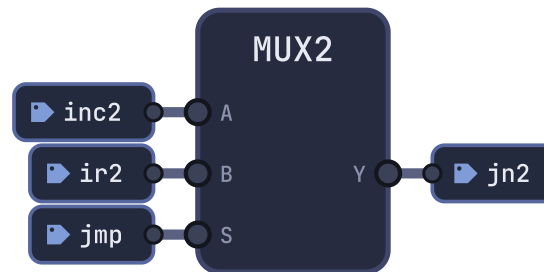
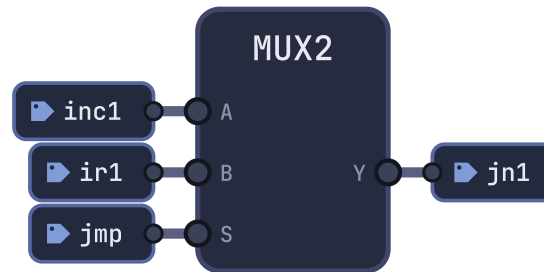
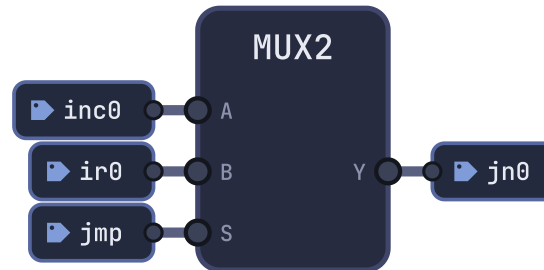
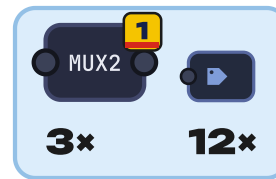
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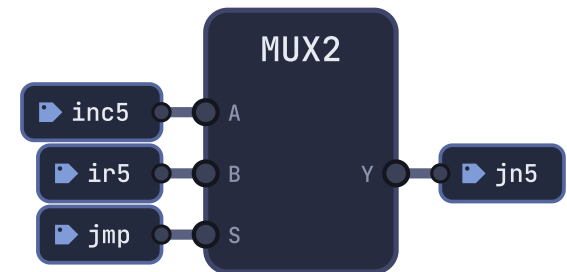
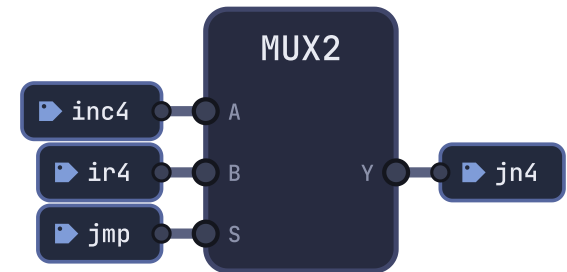
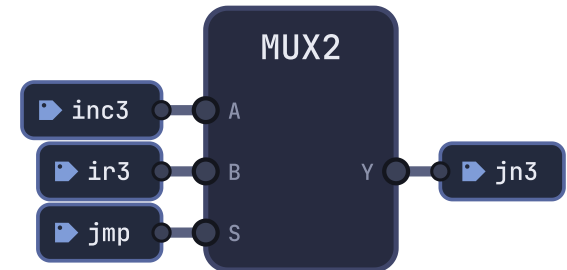
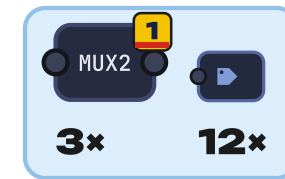
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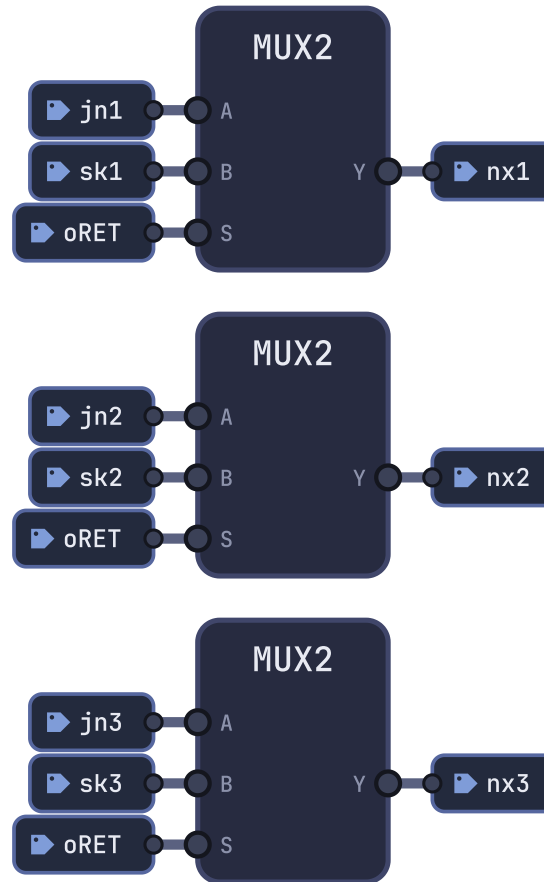
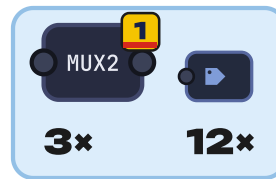
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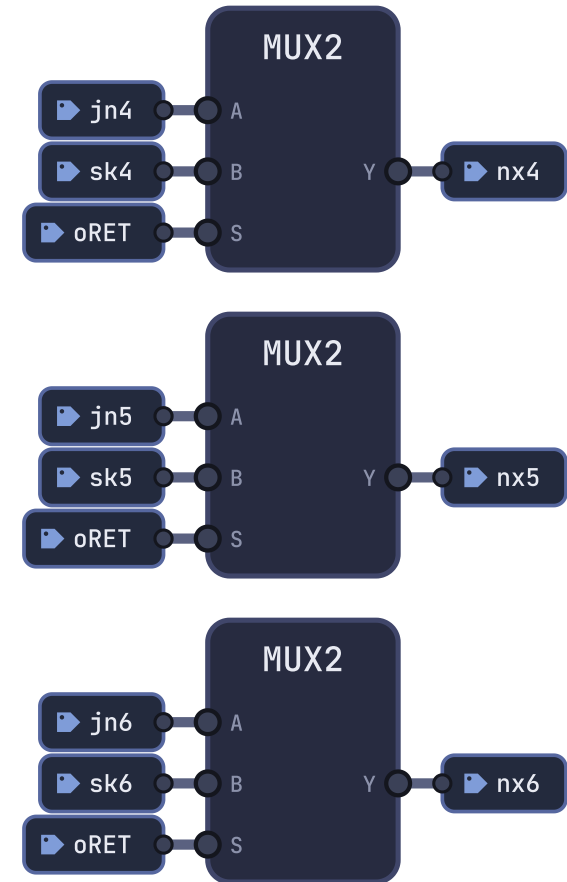
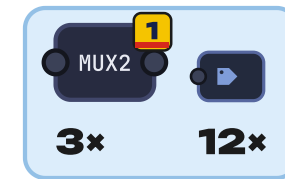
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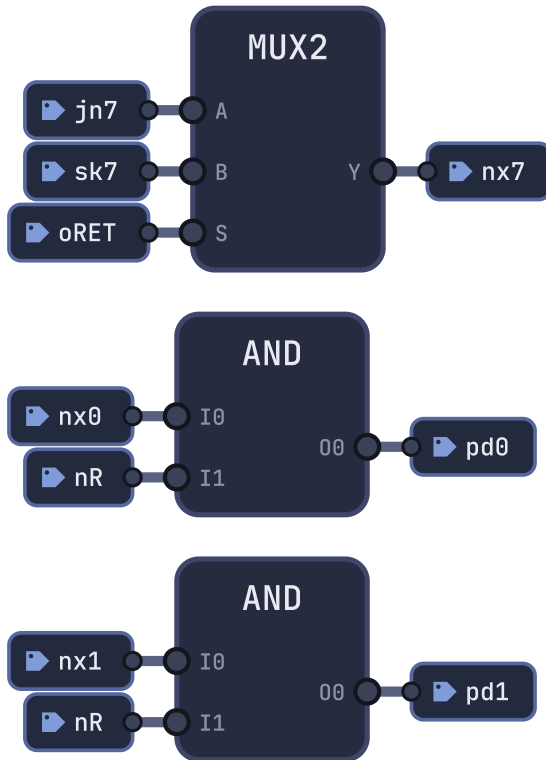
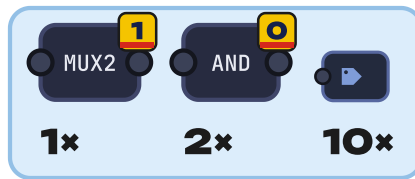
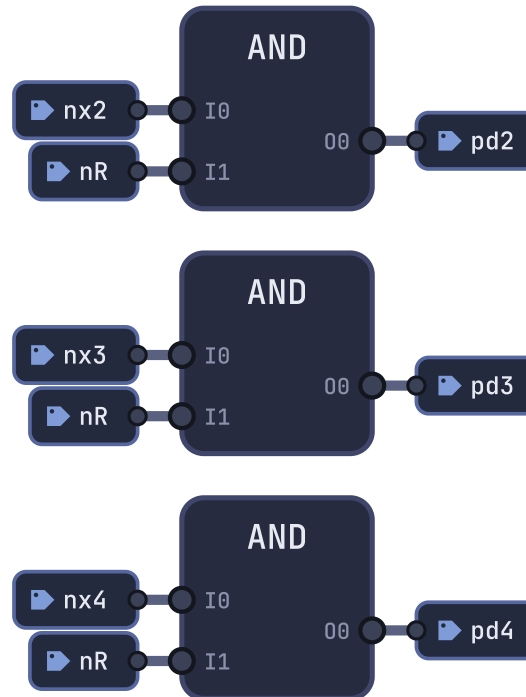
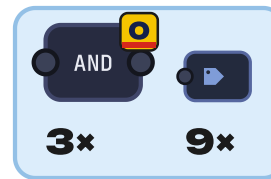
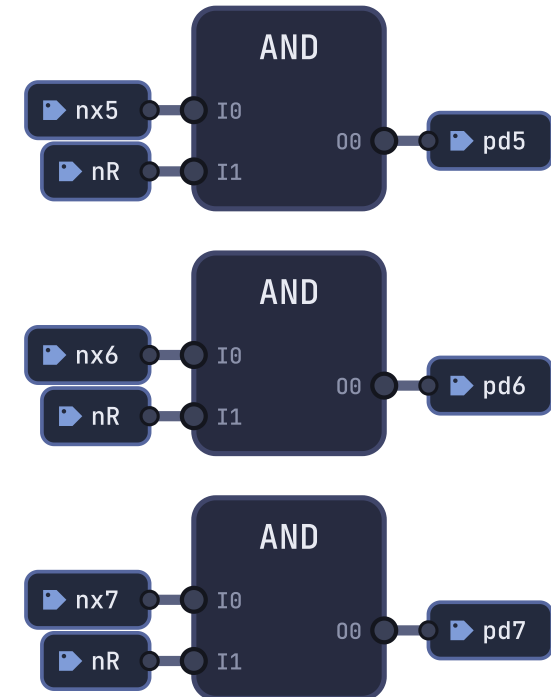
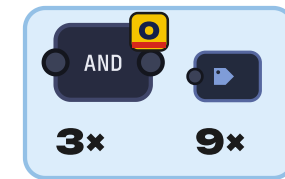


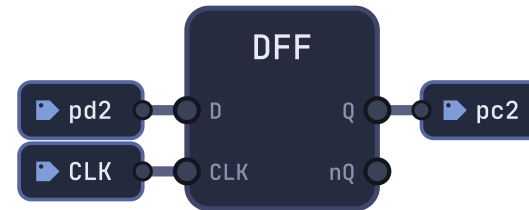
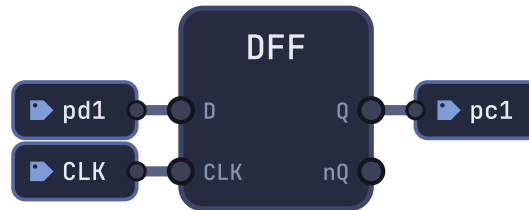
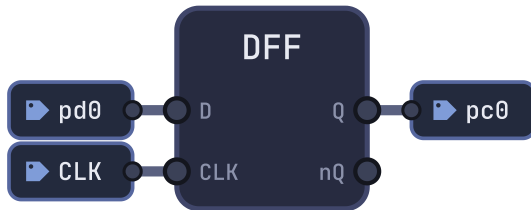
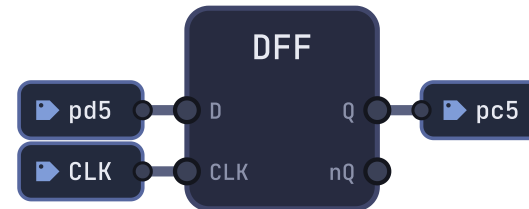
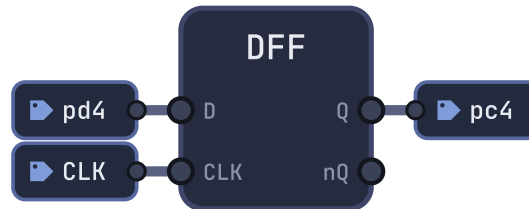
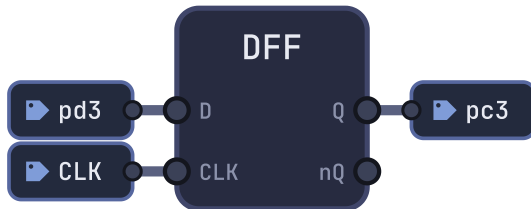
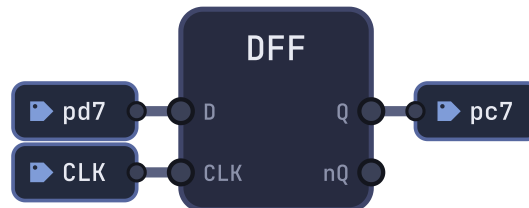
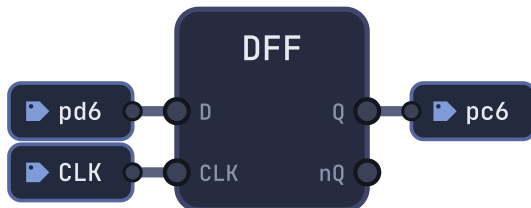
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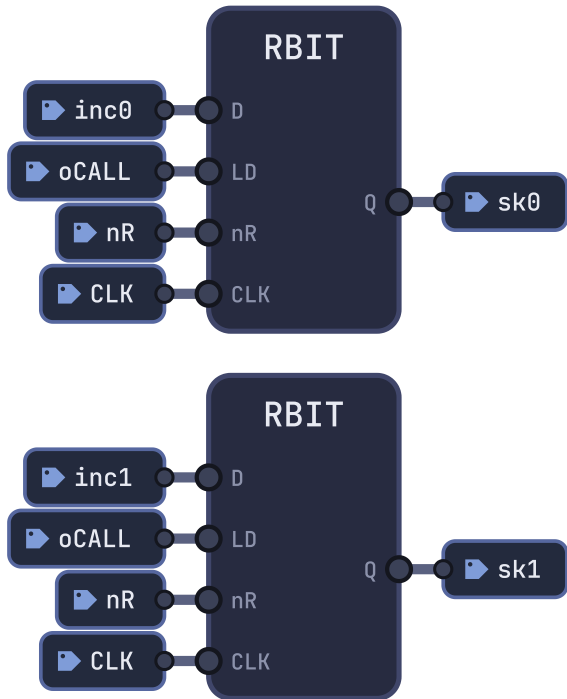
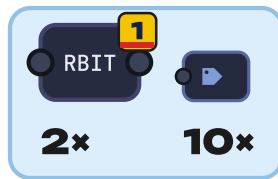
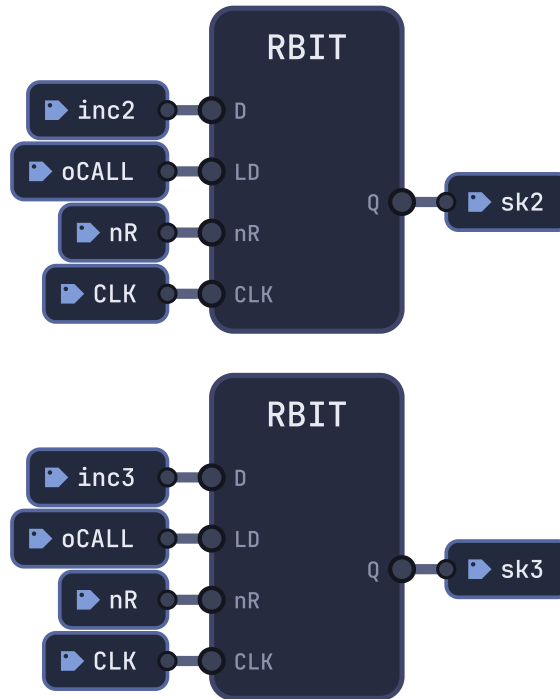
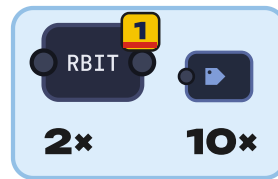
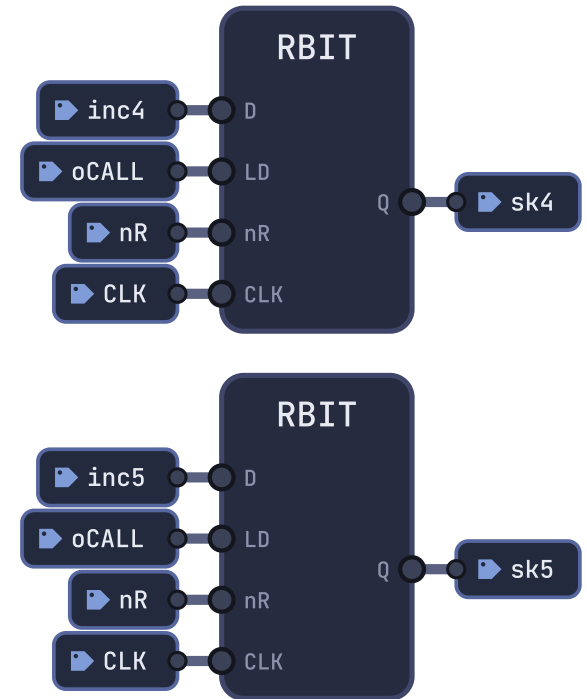
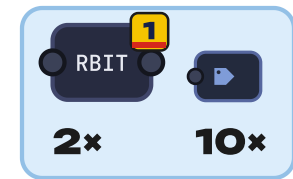


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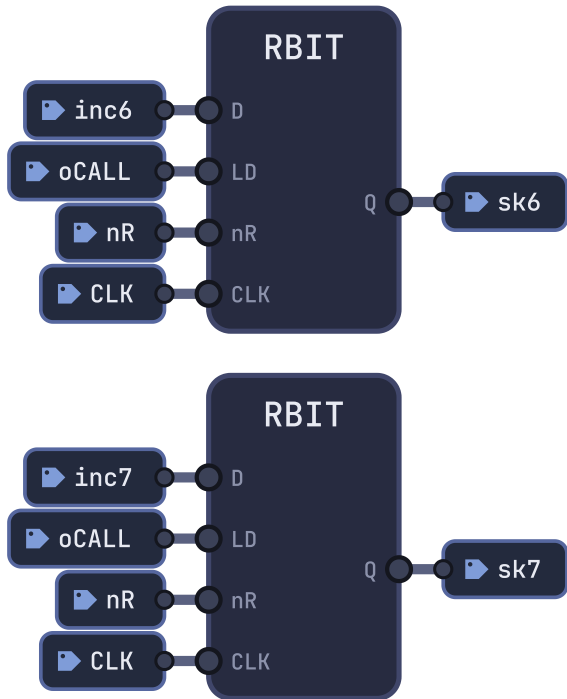
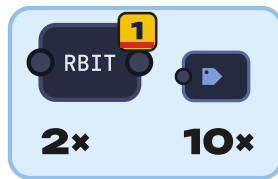


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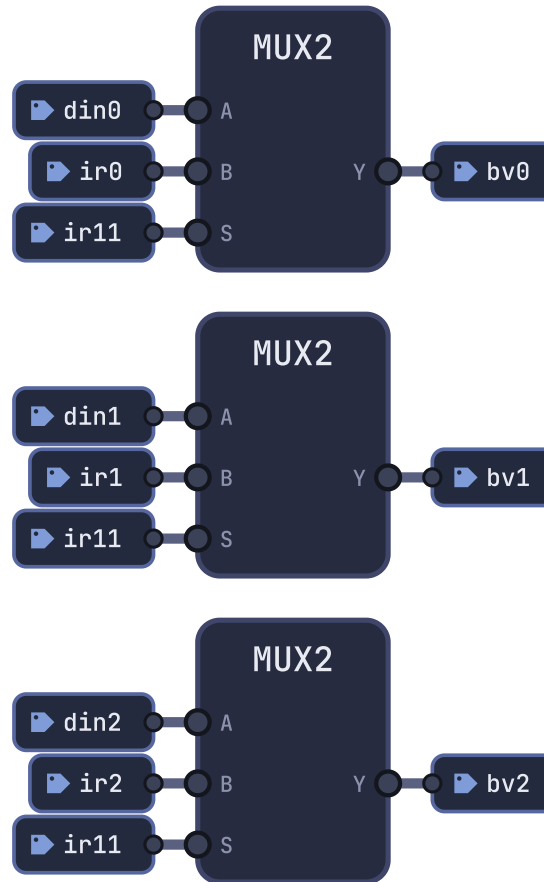
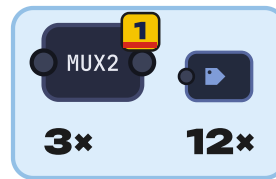
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28**29****30**

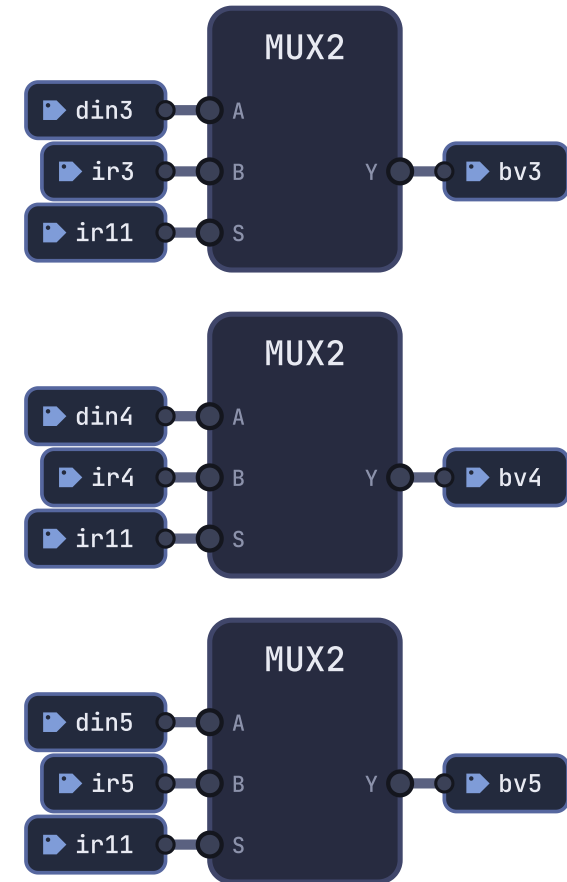
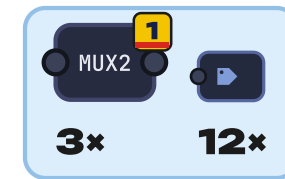
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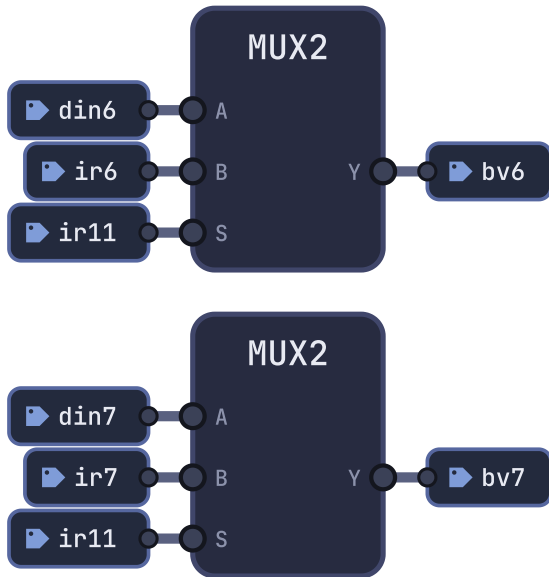
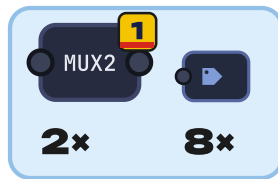
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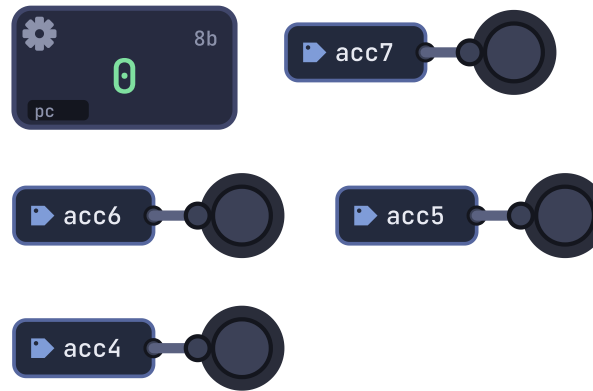
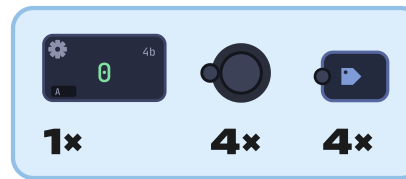
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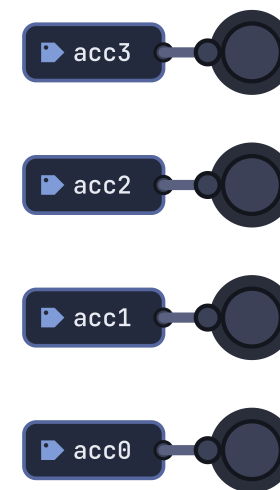
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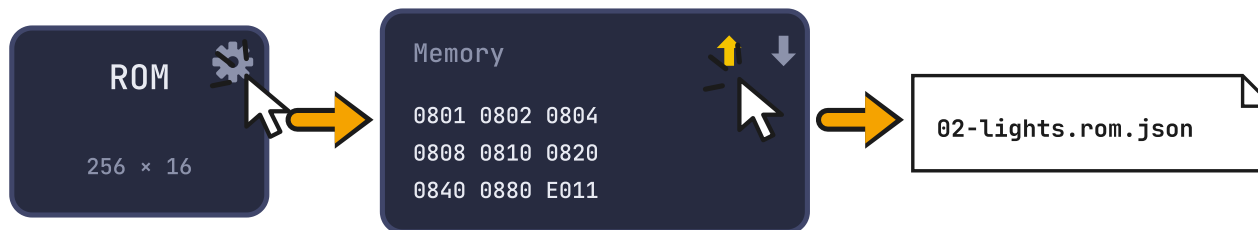
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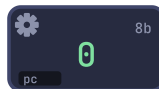
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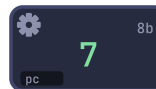
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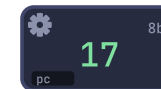
1 → 0 >



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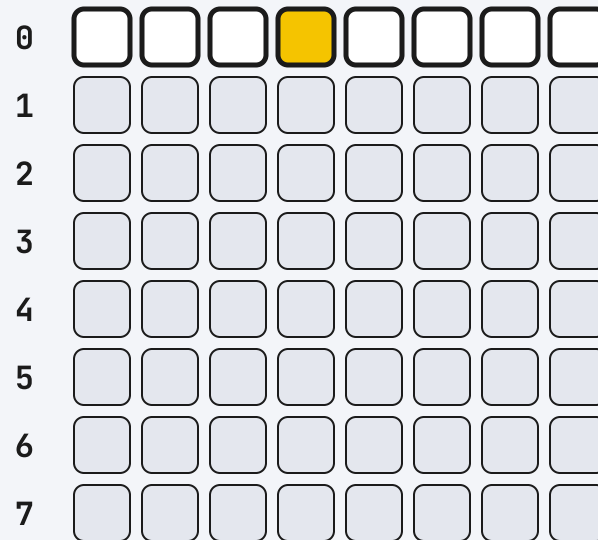
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RAM from latches

8 memory cells and room for the personal data

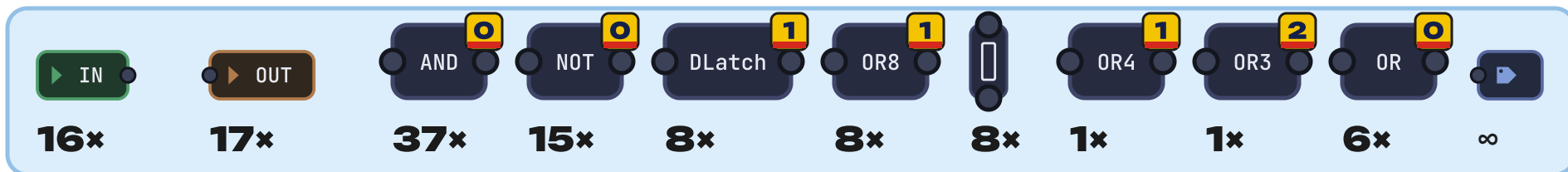


STO

A → cell 0

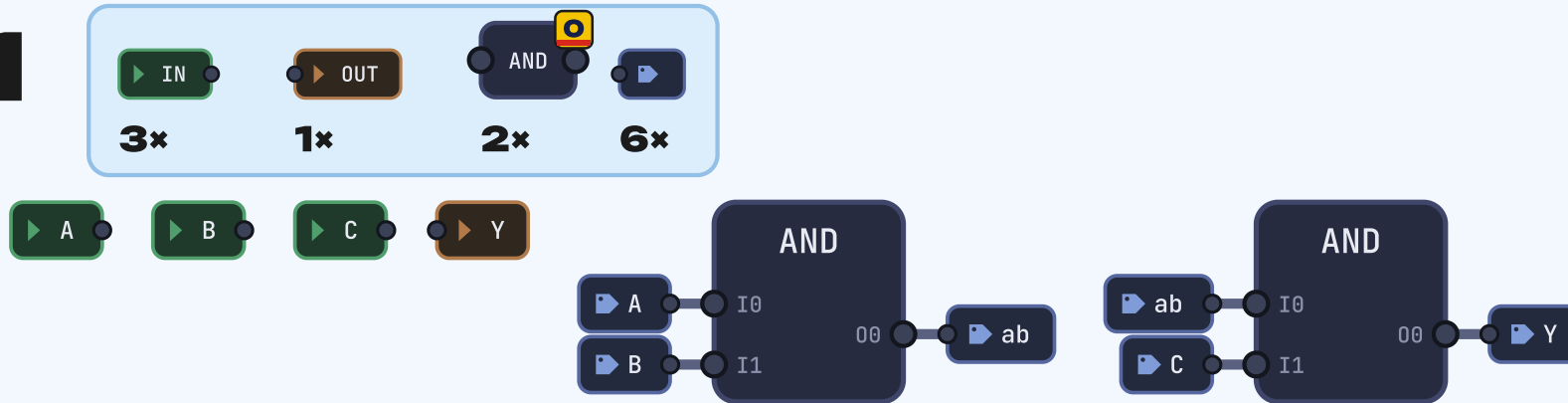
ADD

A + cell 0

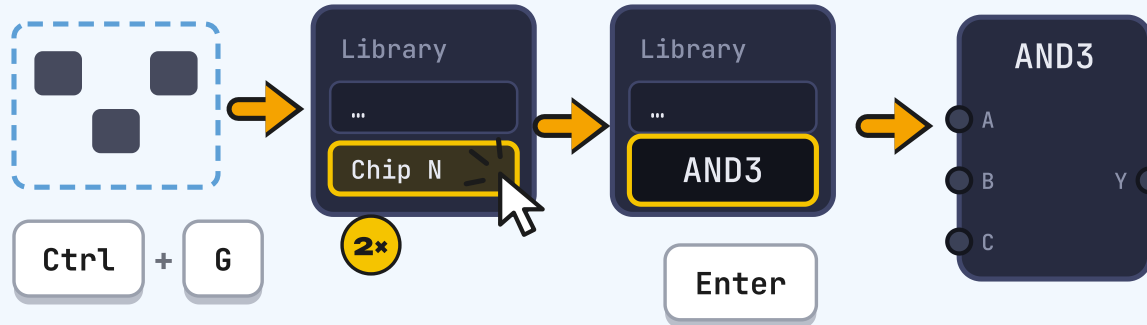


AND3

1

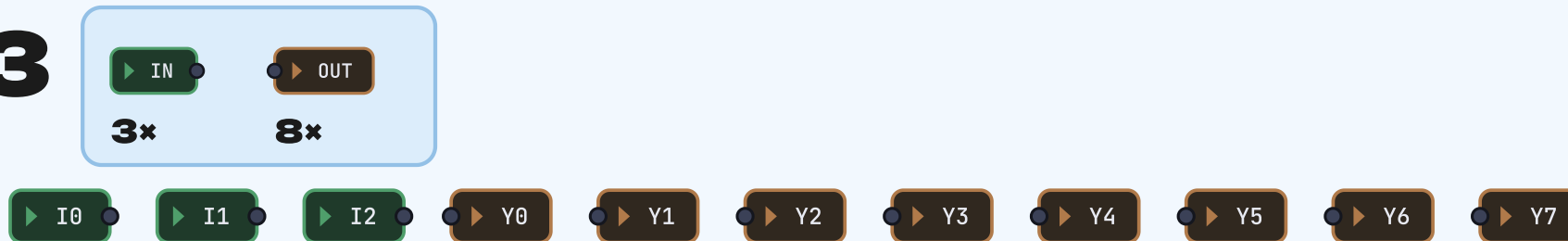


2



DEC8

3



4

NOT

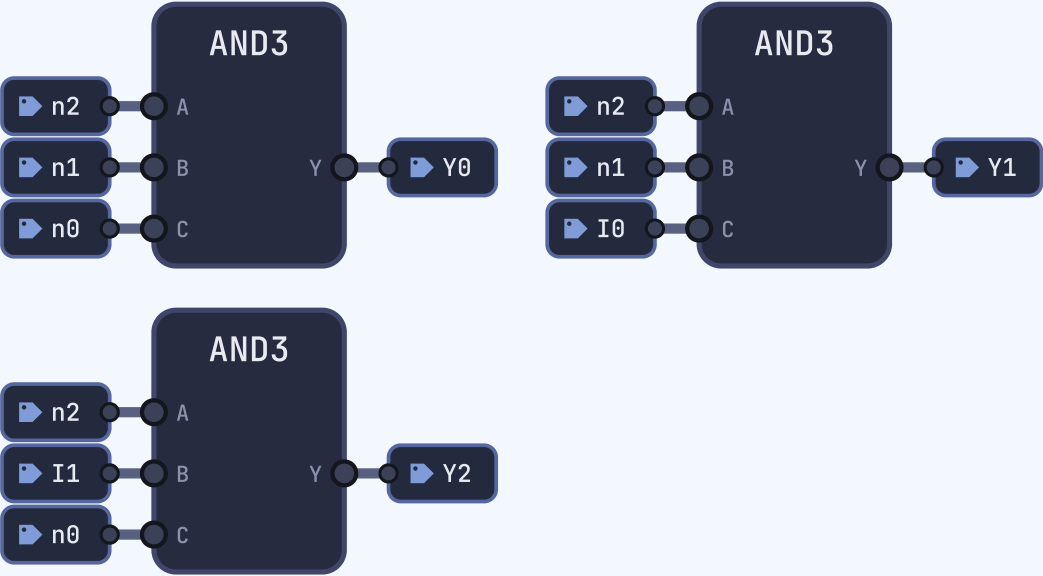
3x 6x



5

AND3

3x 12x

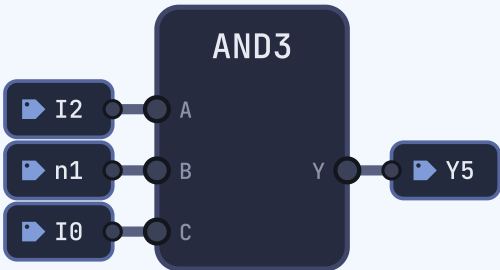
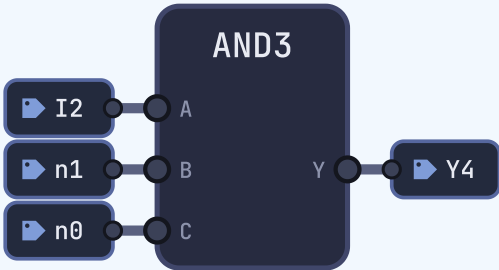
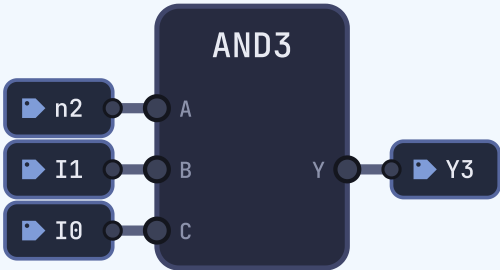


DEC8 ...

6

AND3

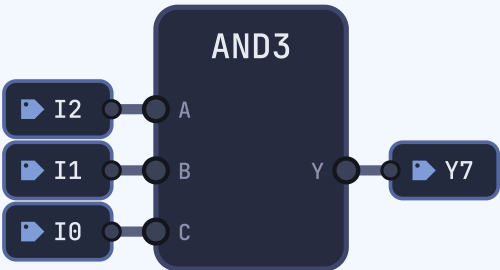
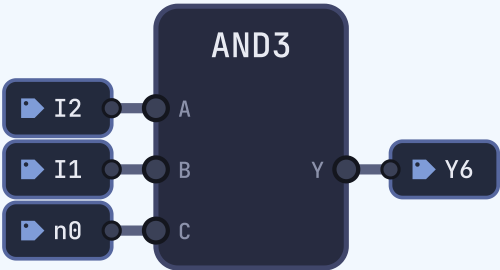
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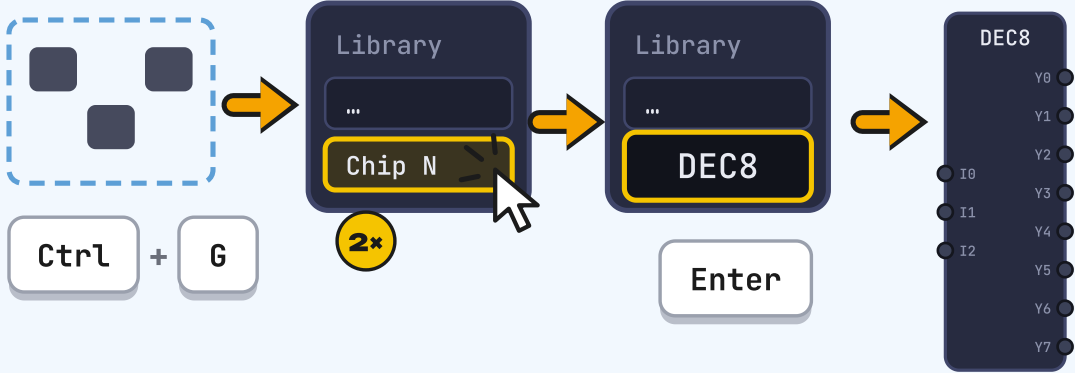
7

AND3

2x8x

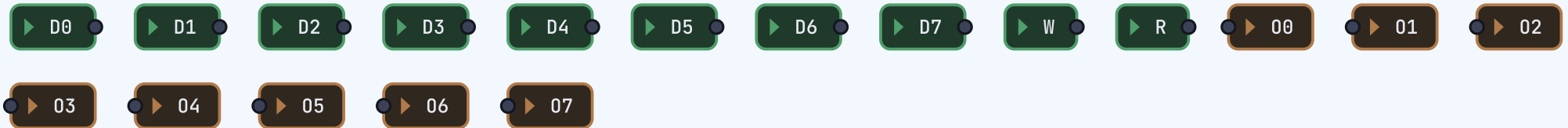
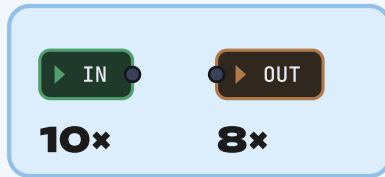


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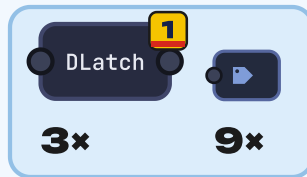


WORDS

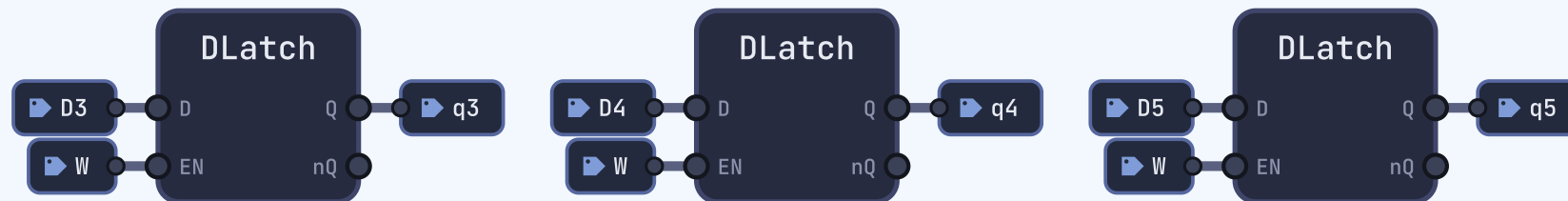
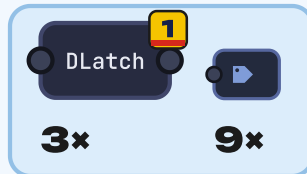
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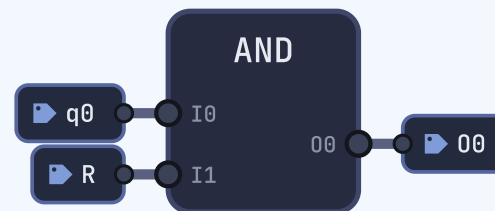
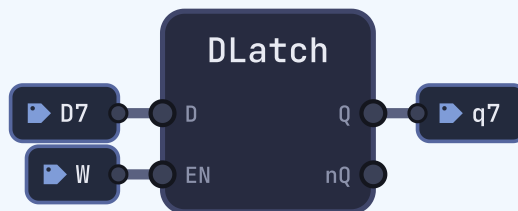
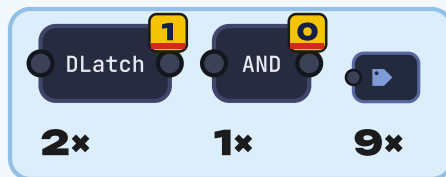
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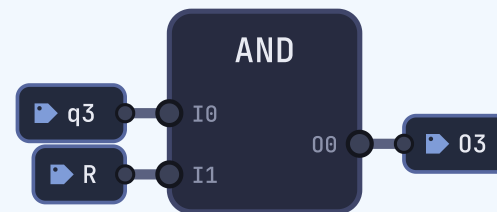
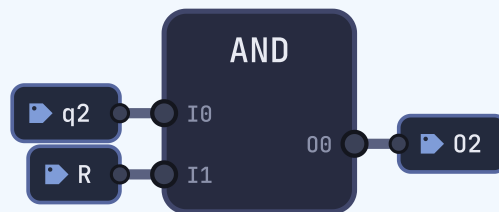
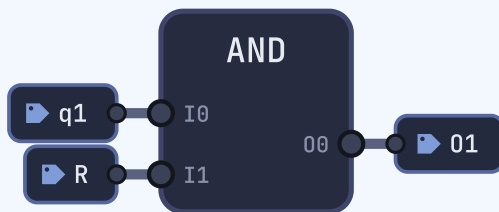
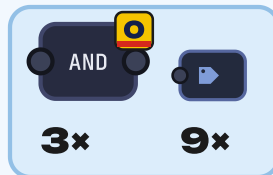
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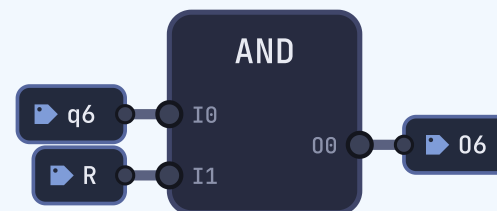
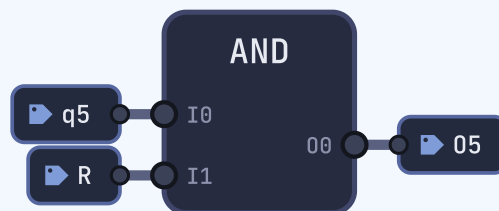
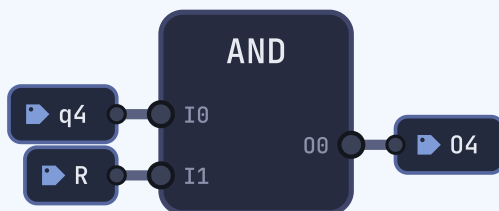
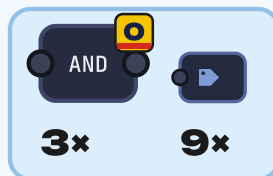
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13

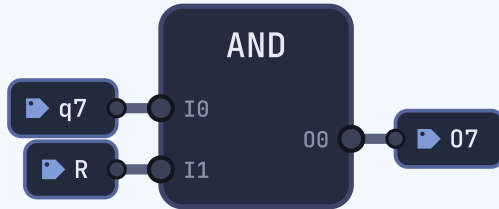


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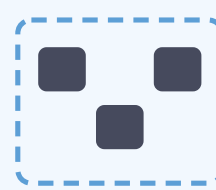


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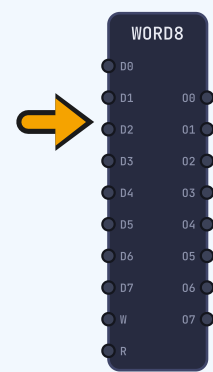
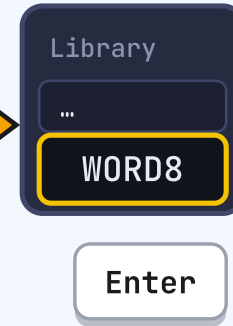
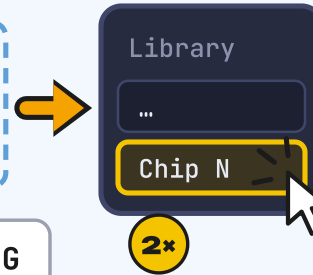
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16

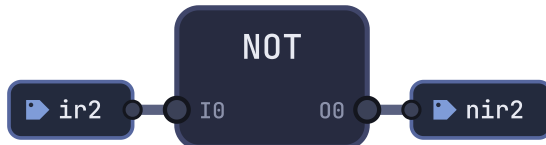
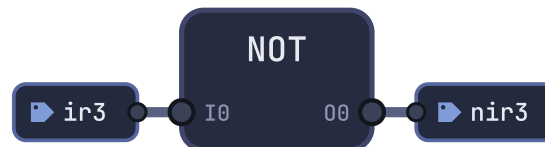
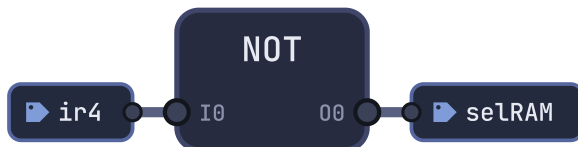


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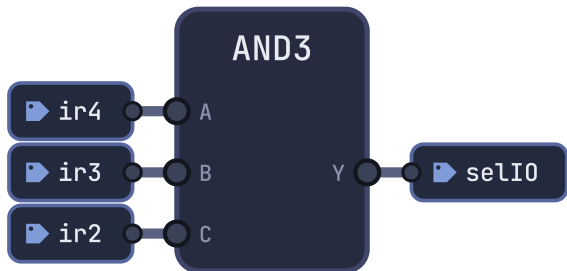
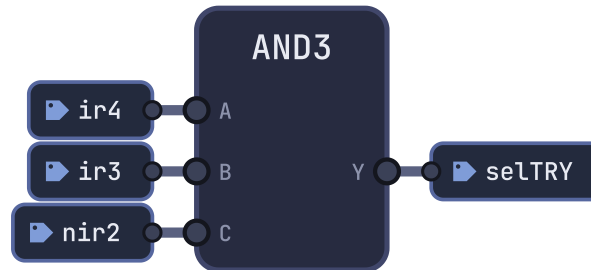
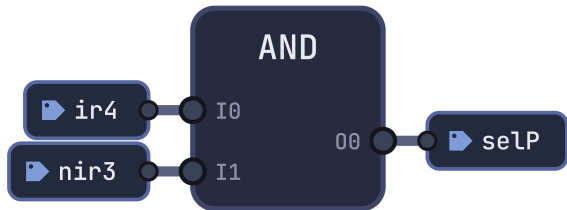


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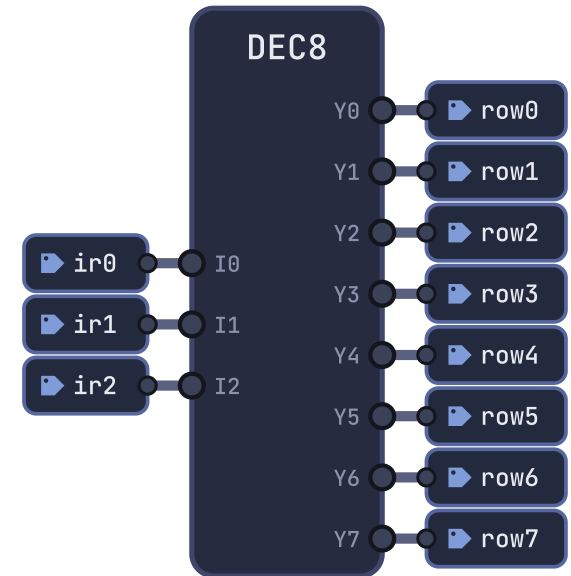
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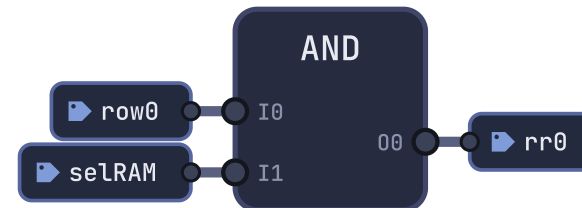
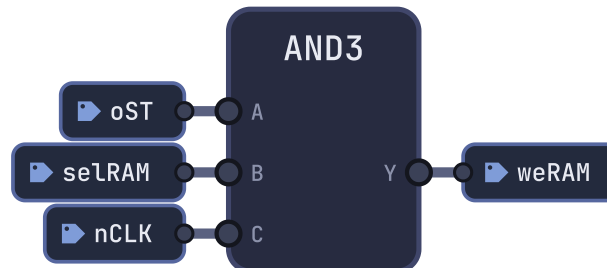
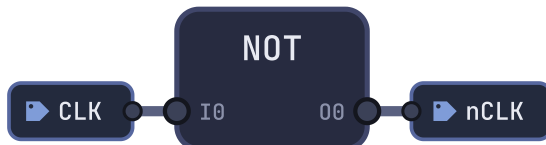
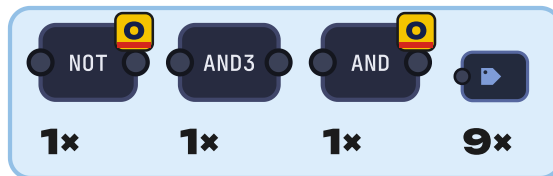
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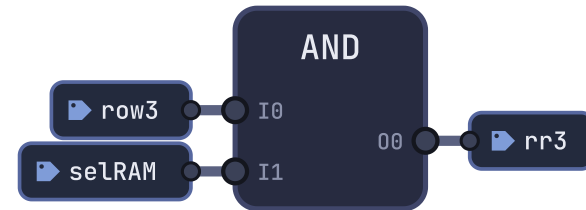
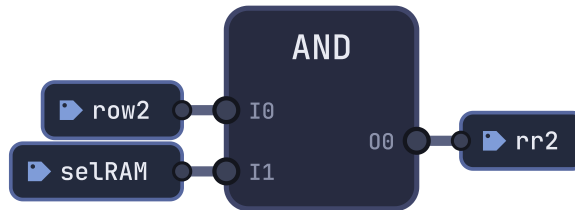
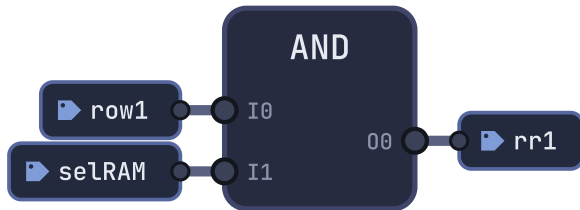
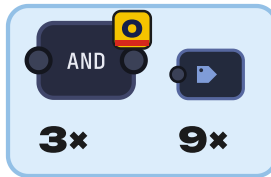
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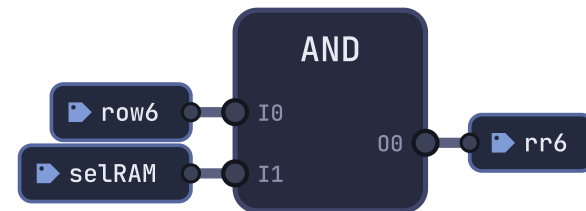
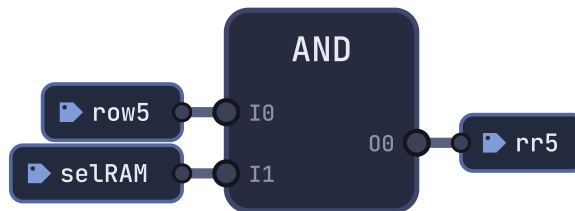
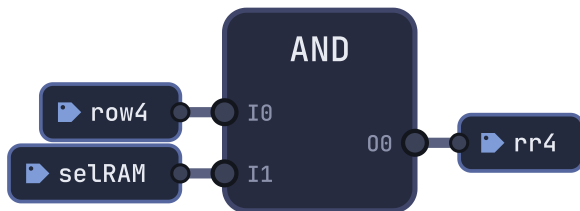
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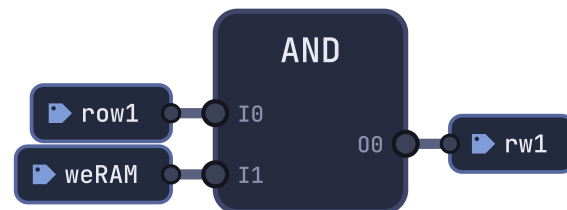
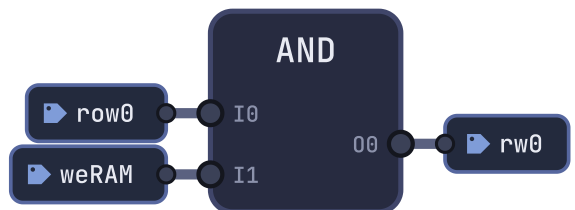
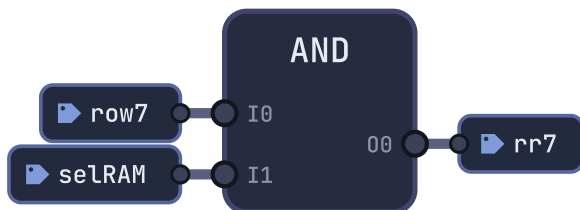
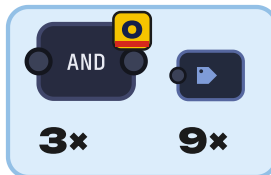
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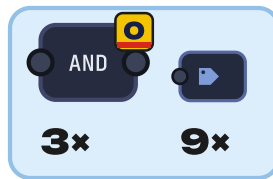
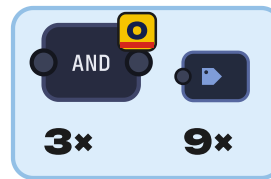
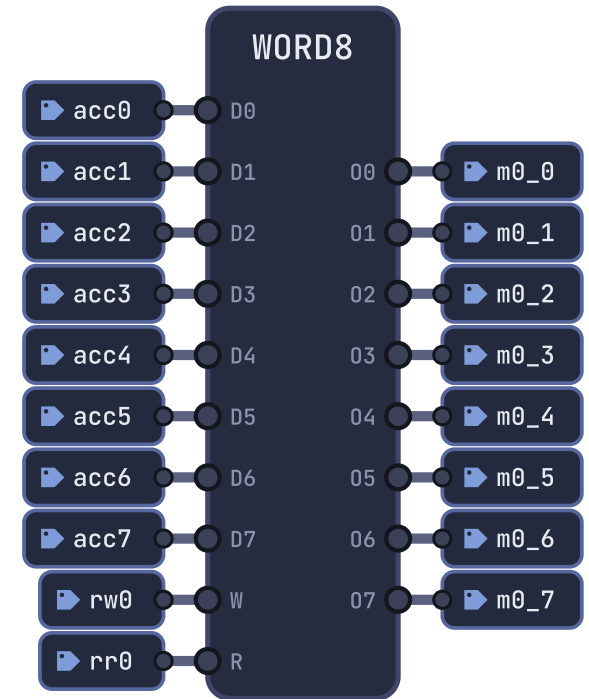
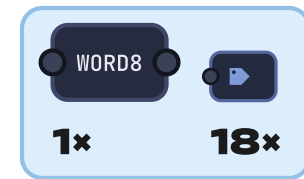


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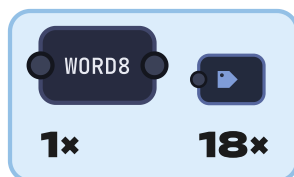


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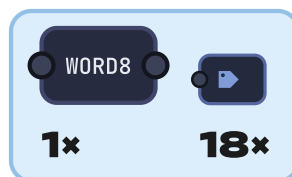


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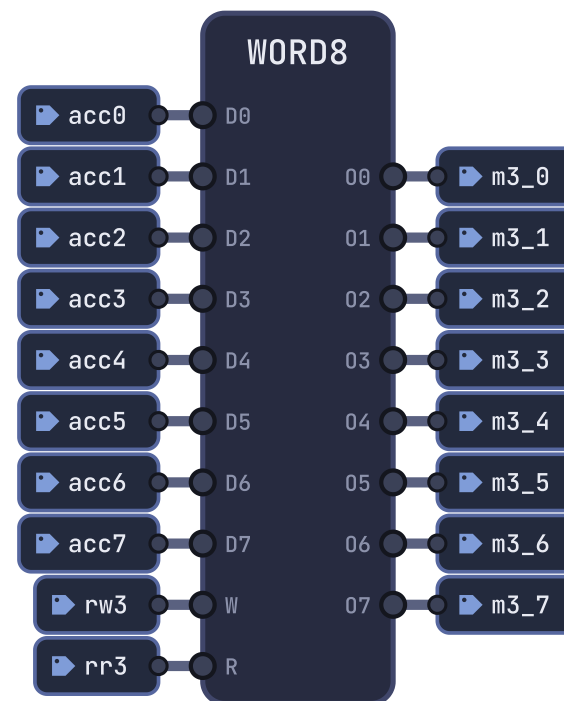
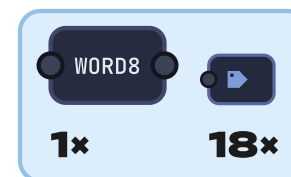
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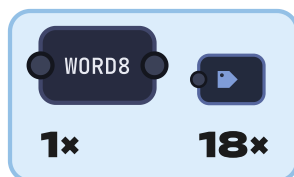
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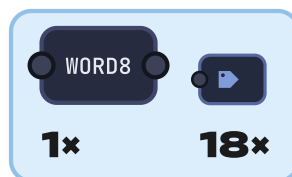
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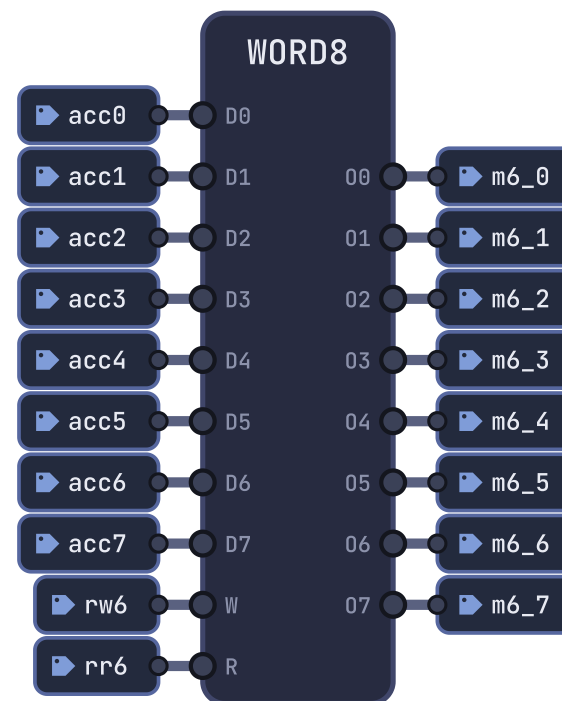
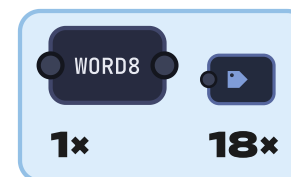
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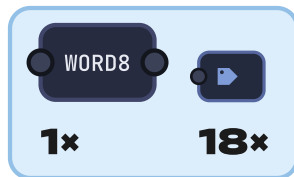
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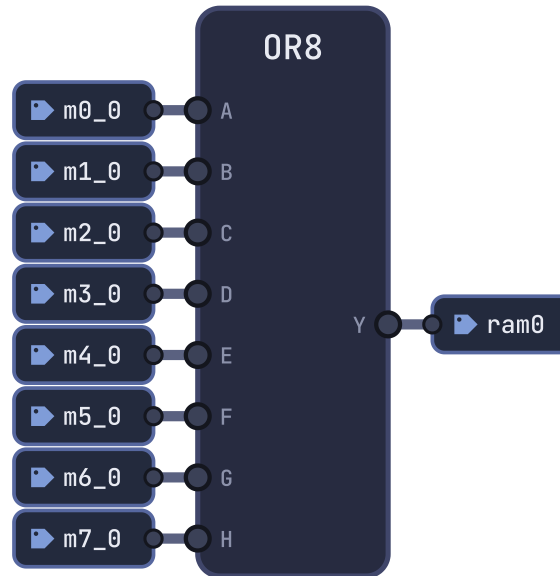
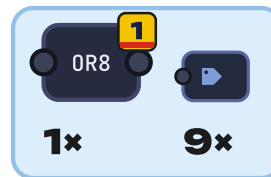
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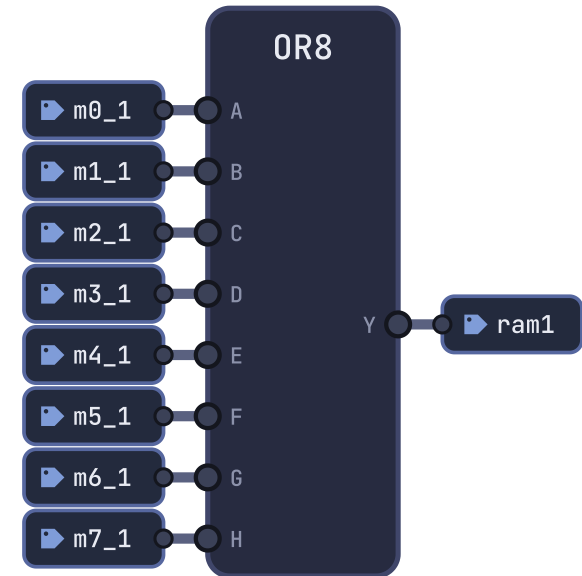
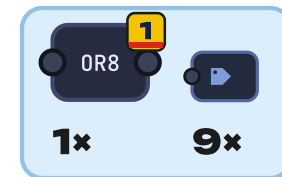
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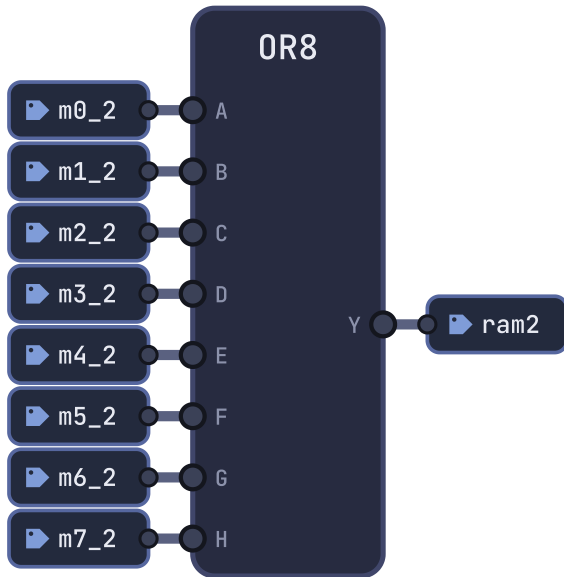
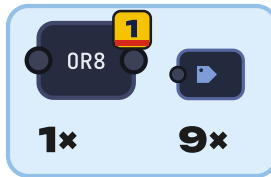
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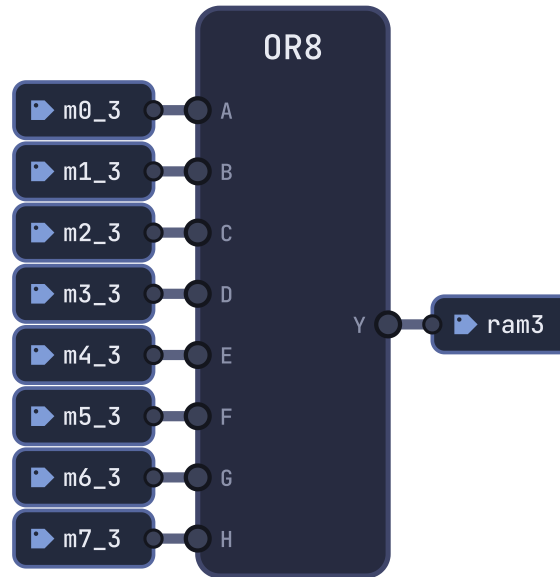
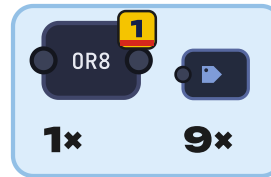
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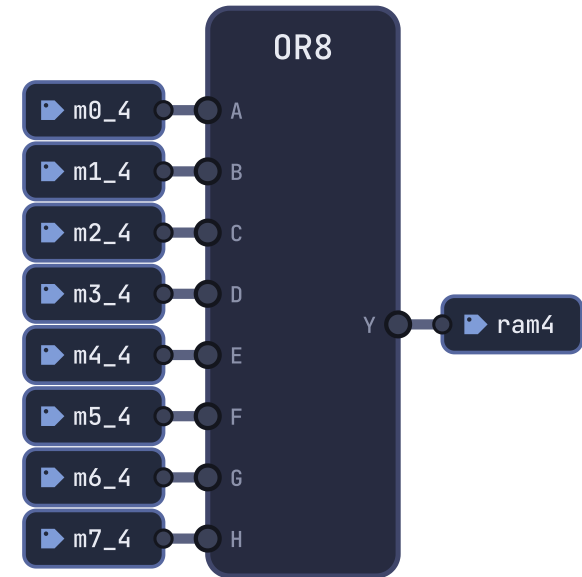
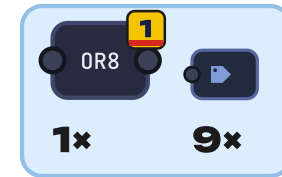
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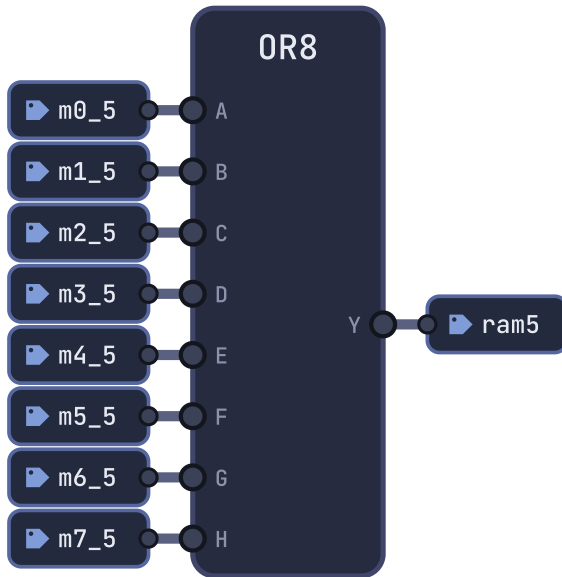
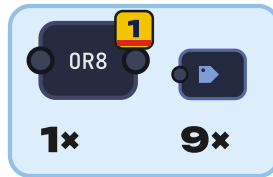
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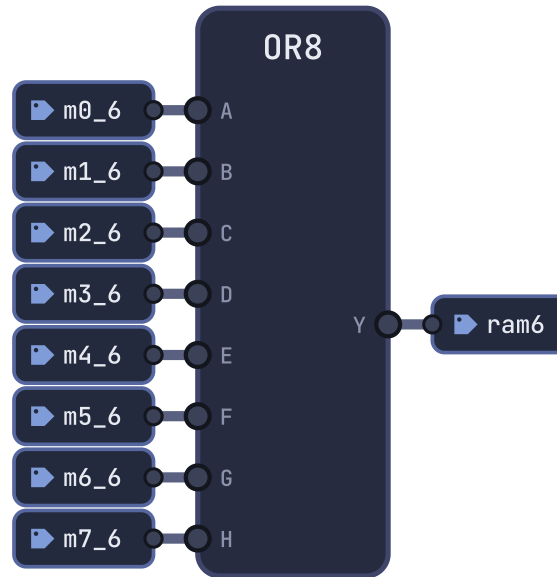
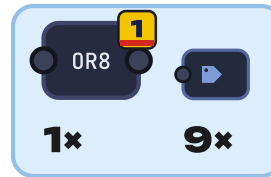
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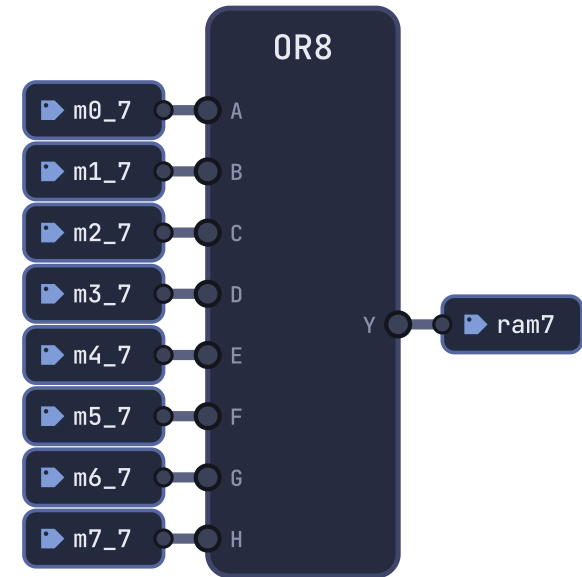
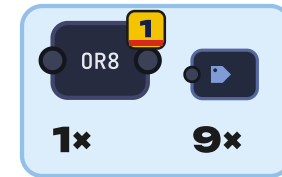
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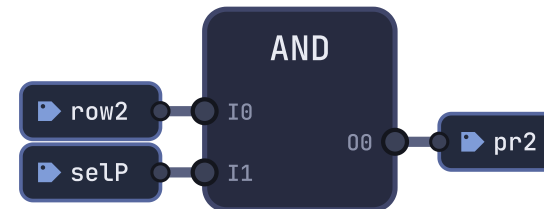
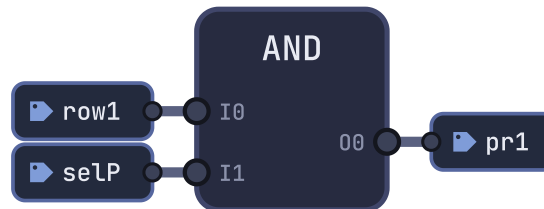
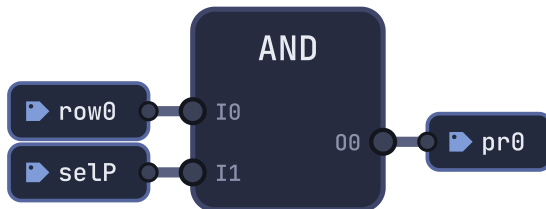
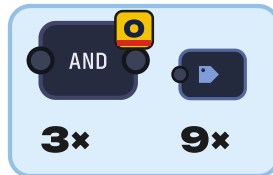
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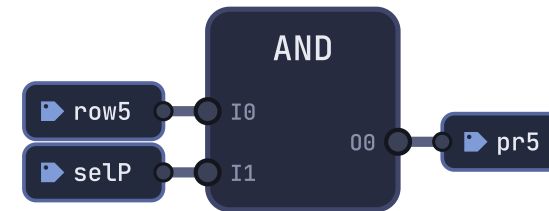
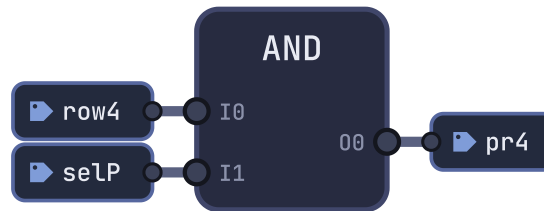
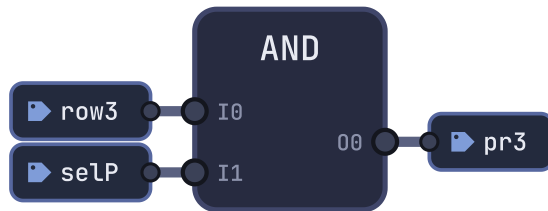
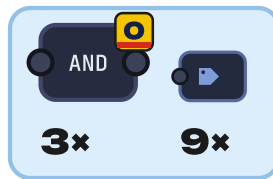
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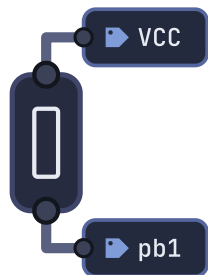
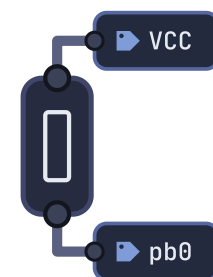
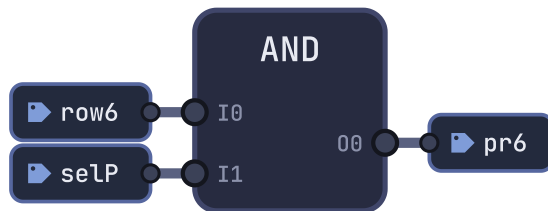
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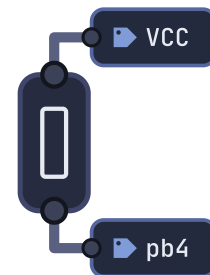
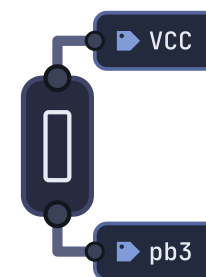
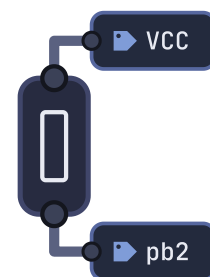
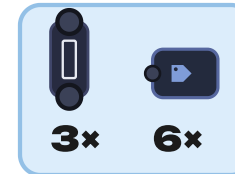
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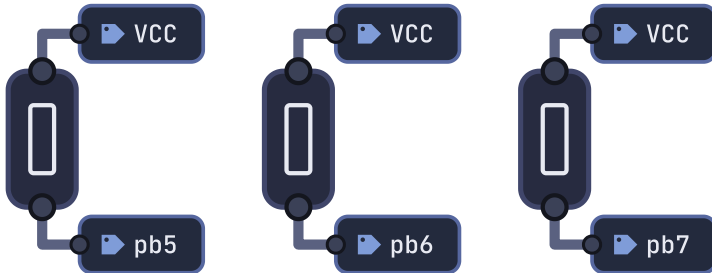
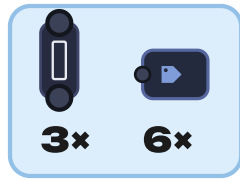
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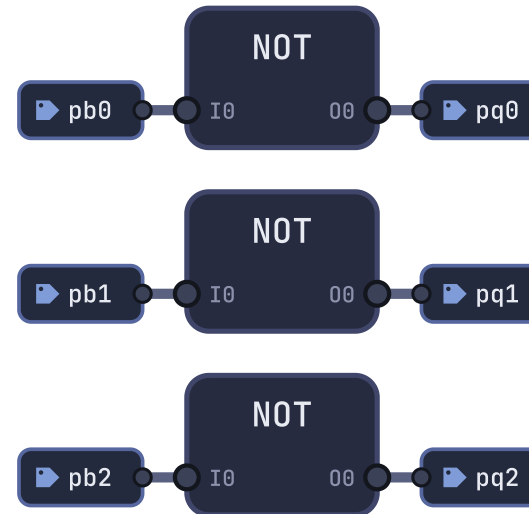
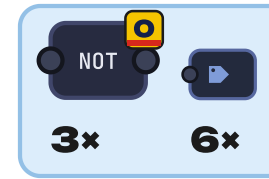
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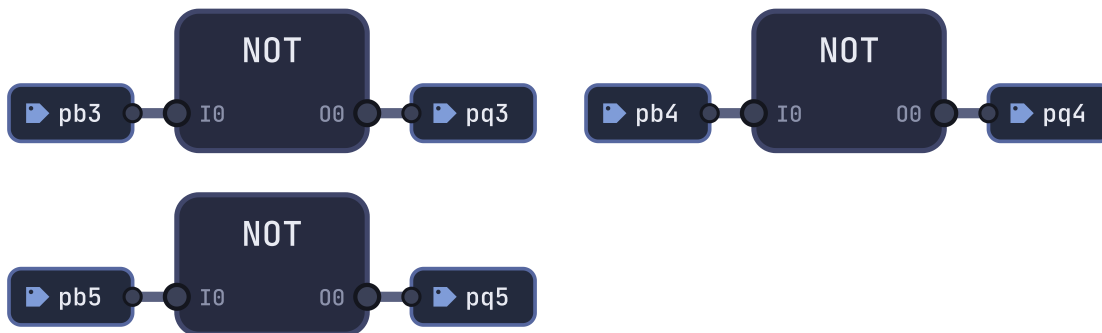
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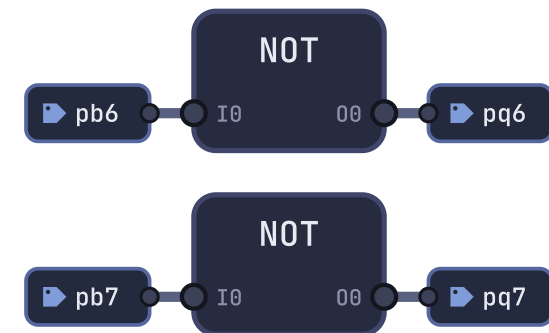
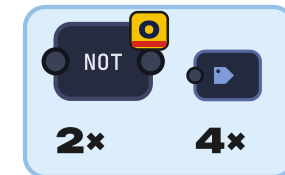
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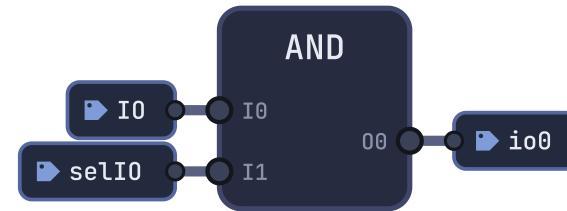
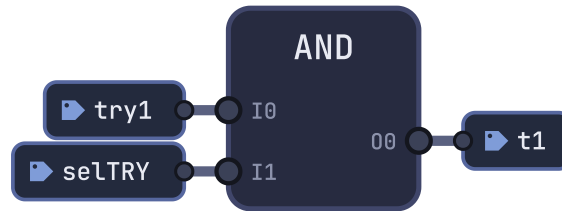
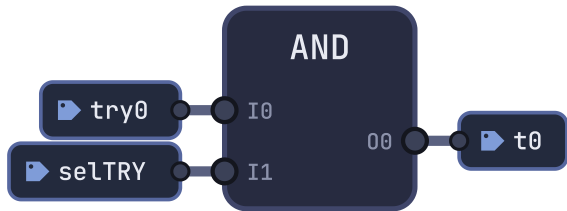
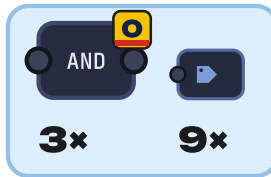
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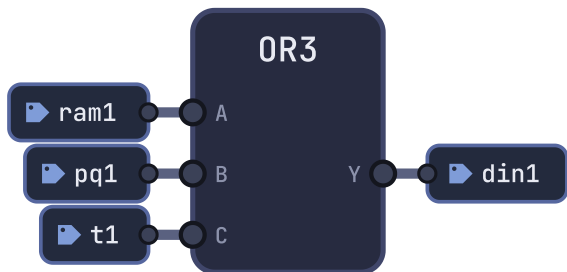
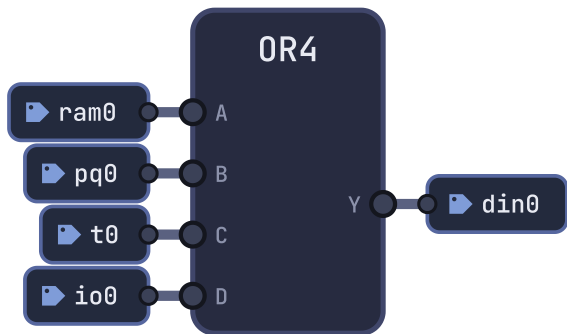
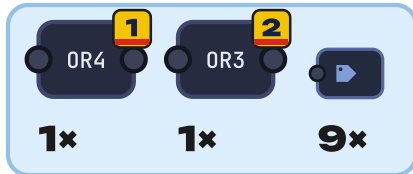
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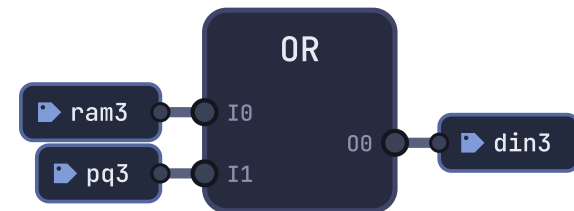
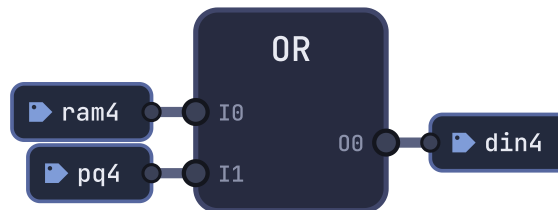
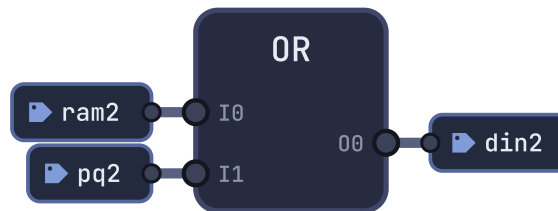
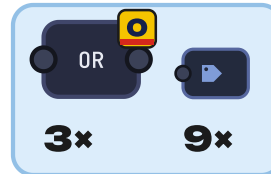
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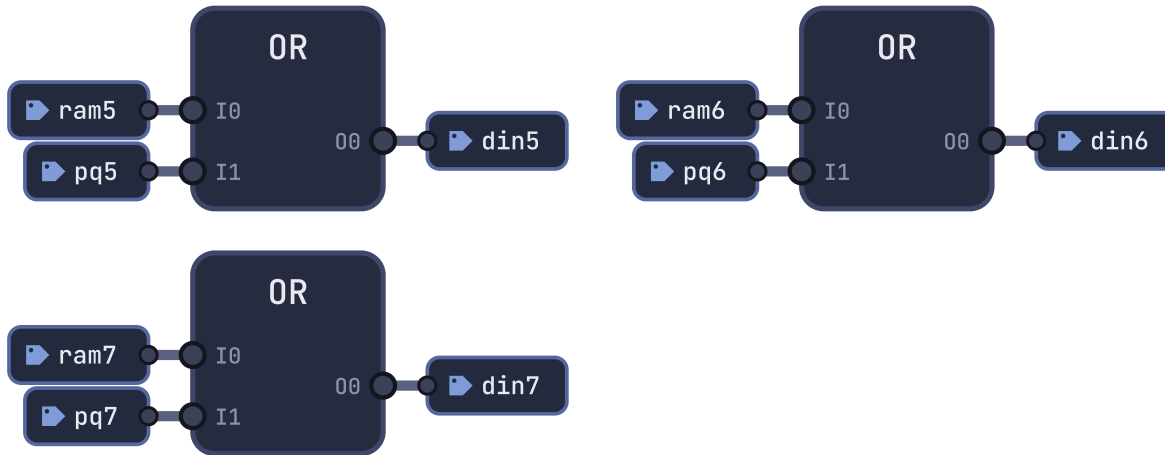
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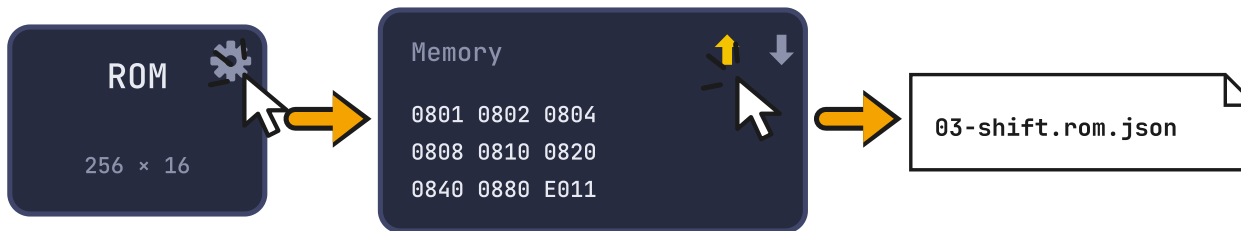
52



53



54



1

2

4

8

128

0

3 x CLK: ST 0 · ADD 0 · JNC



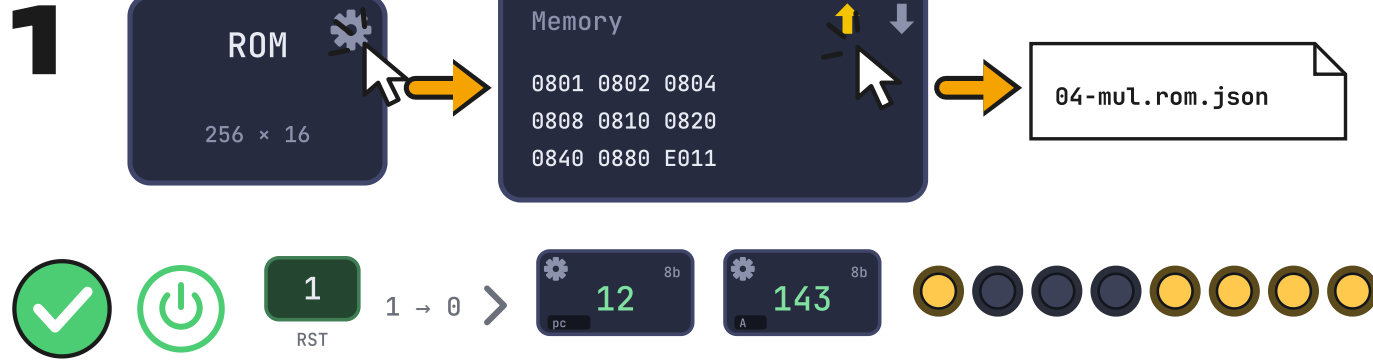
Loops and conditions

no new parts: 13×11 by repeated addition

$$13 \times 11$$

$13 + 13 + \dots + 13$ (11 times)







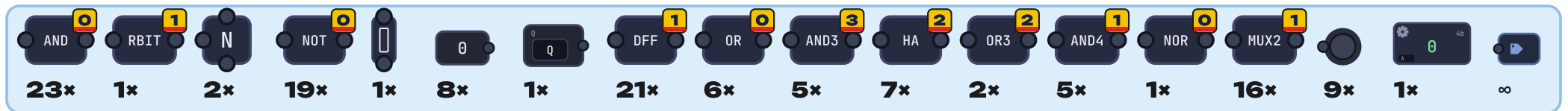
The IO wire and the tester

kh HT-01

a byte bit by bit over one wire

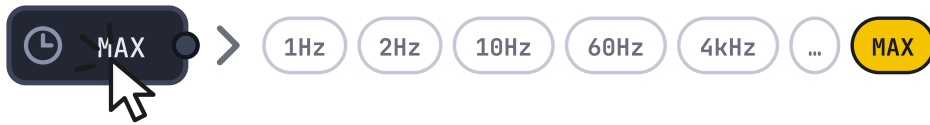


65 → card → 66

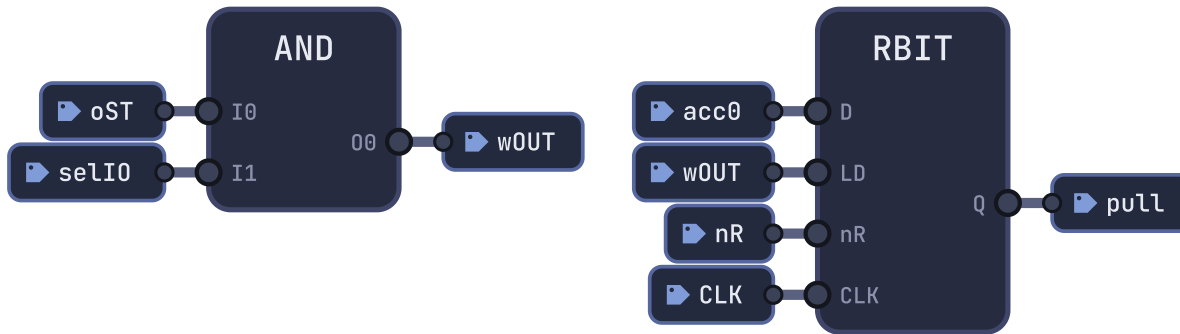


CANVAS

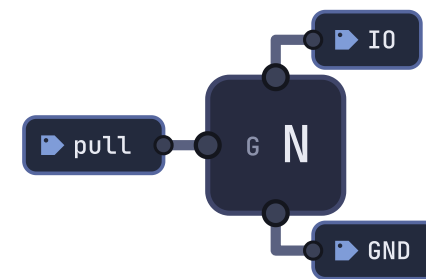
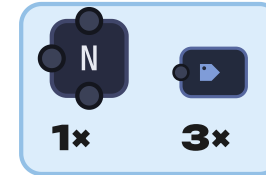
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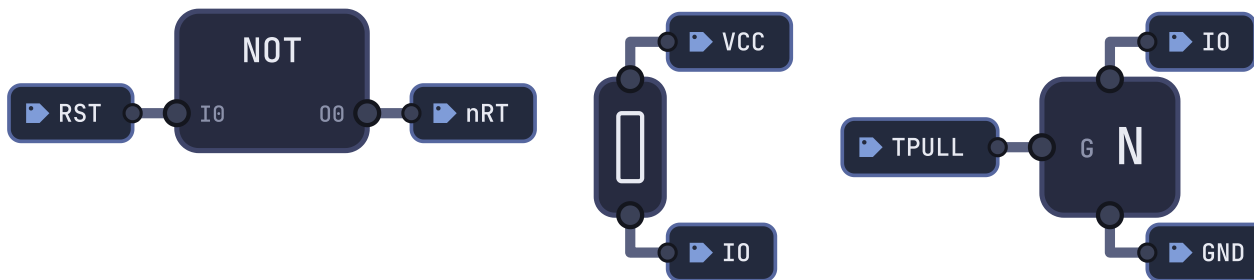
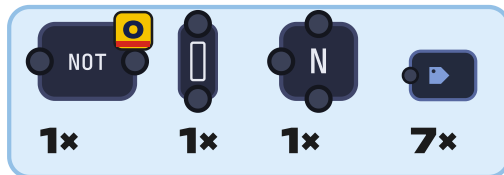
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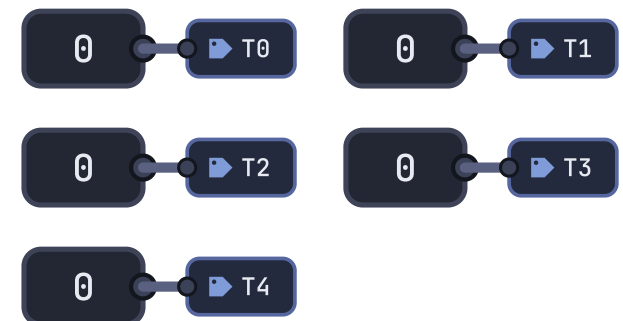
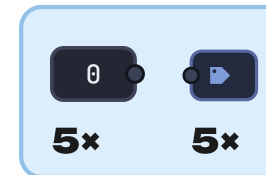
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4

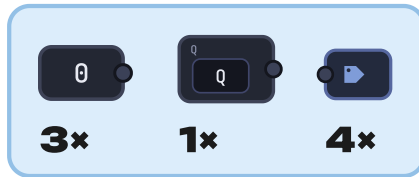


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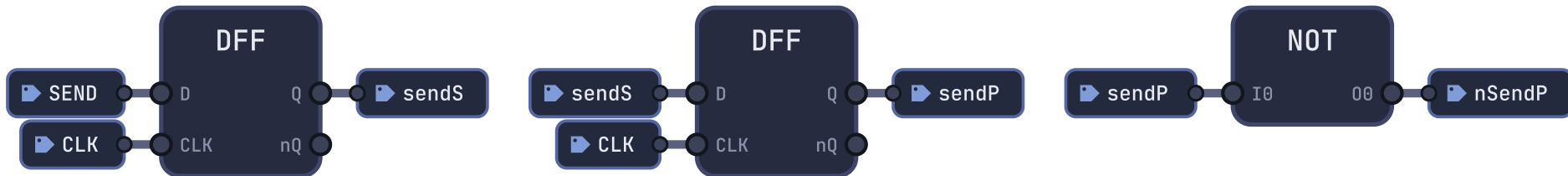
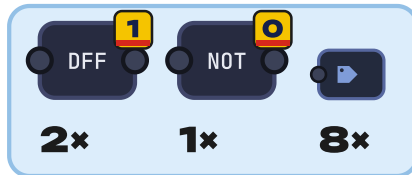


CANVAS ...

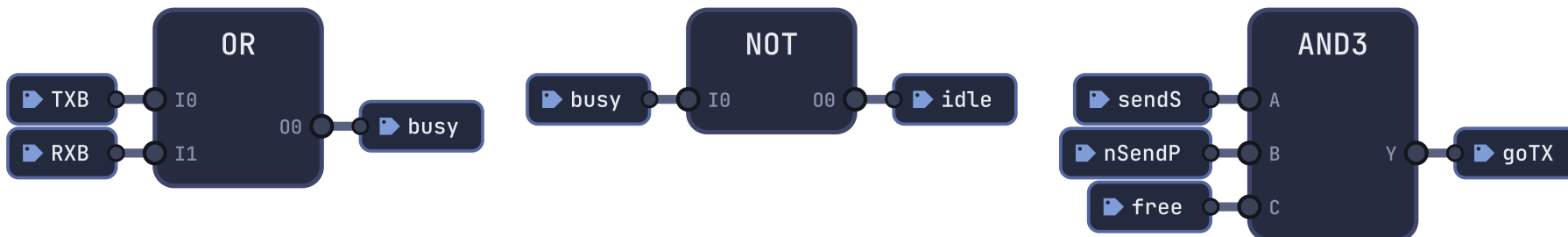
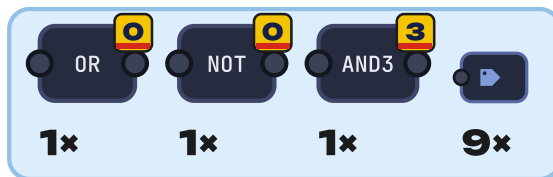
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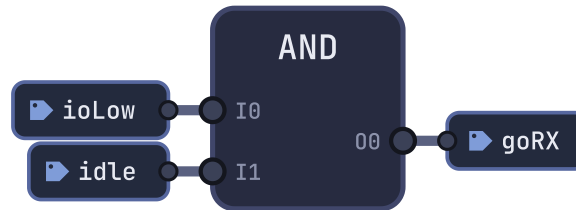
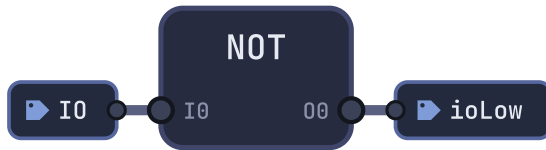
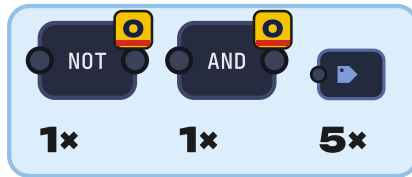
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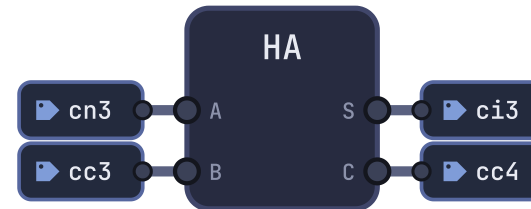
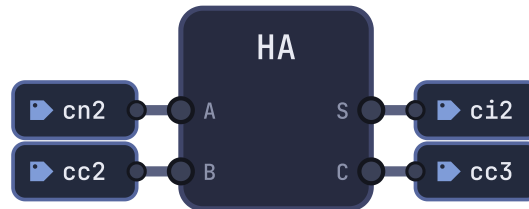
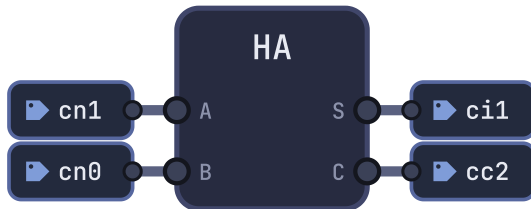
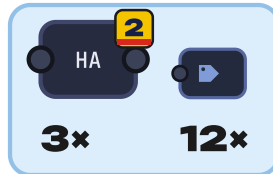
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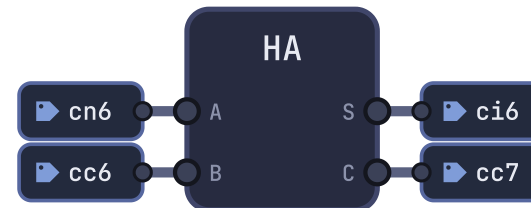
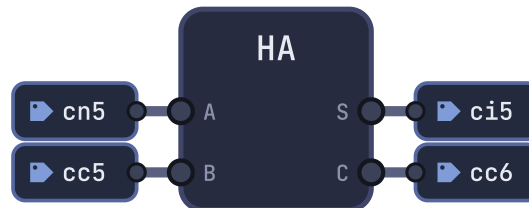
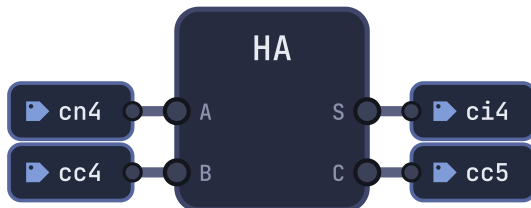
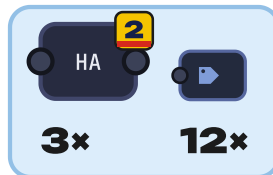
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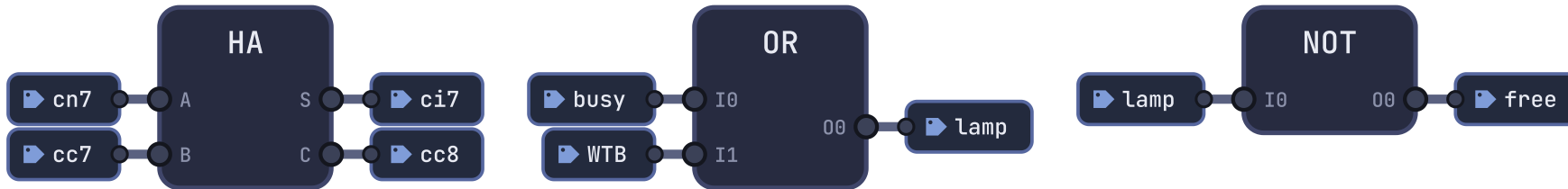
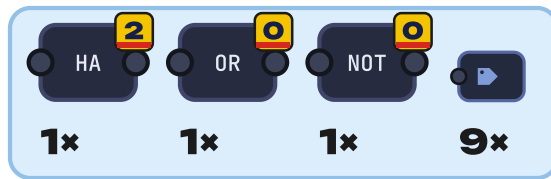
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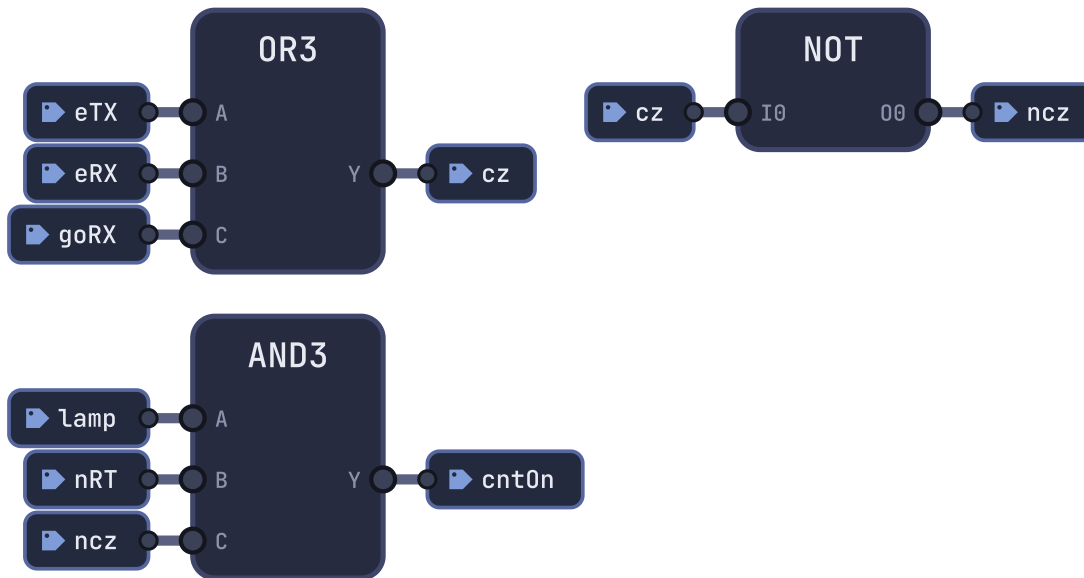
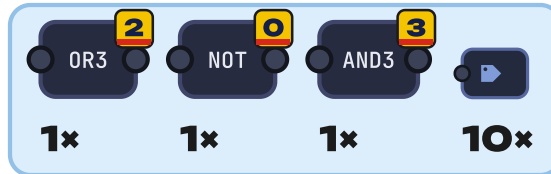
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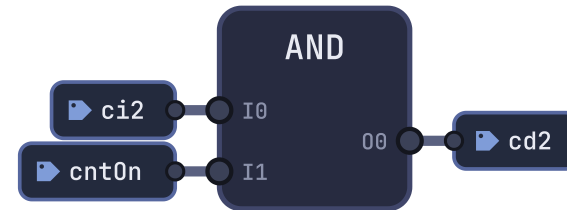
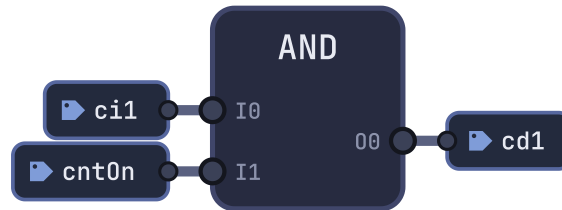
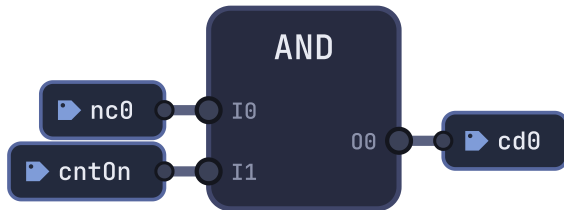
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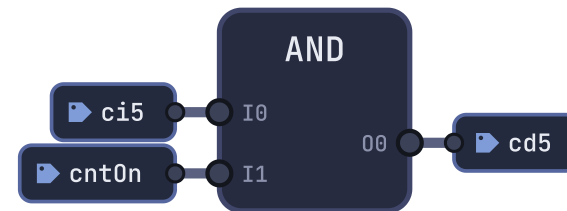
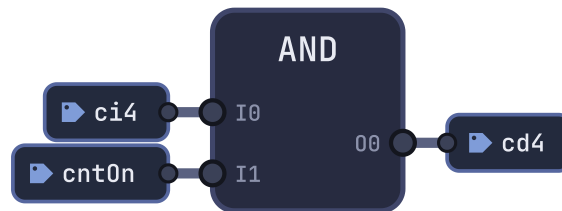
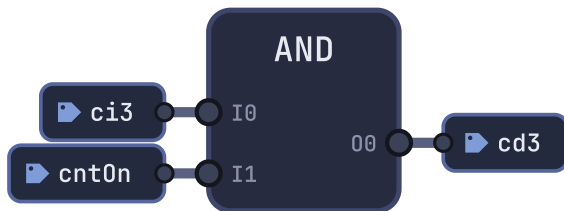
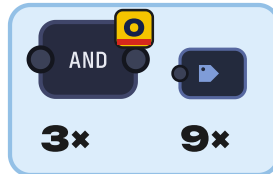
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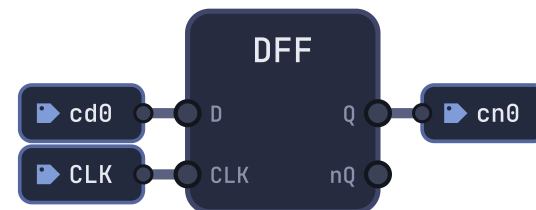
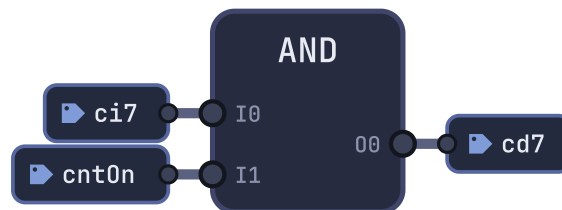
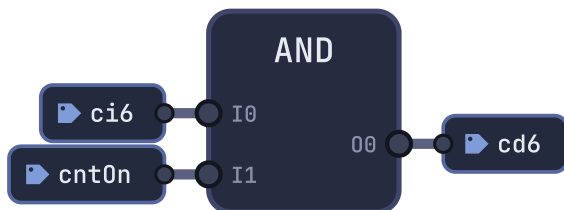
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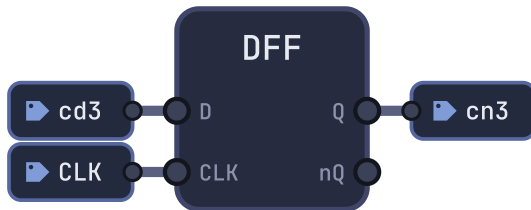
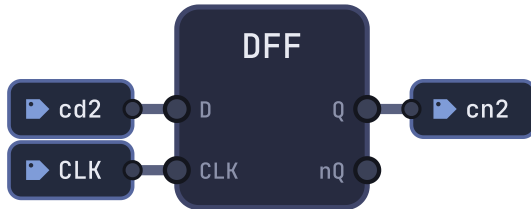
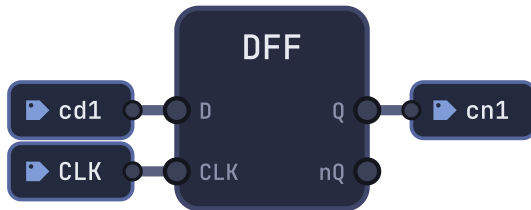
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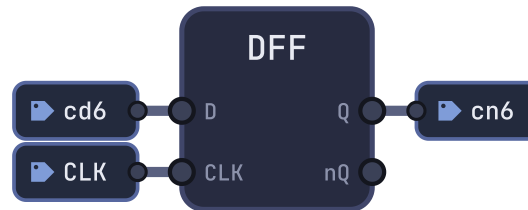
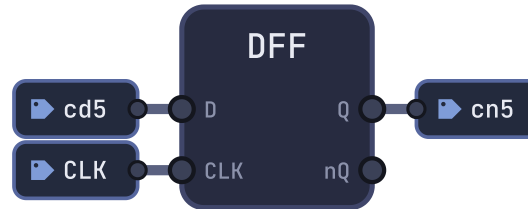
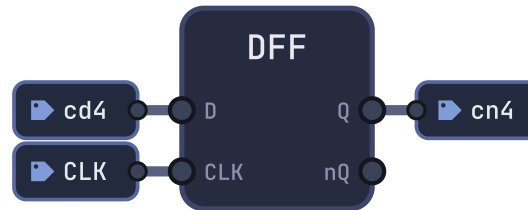
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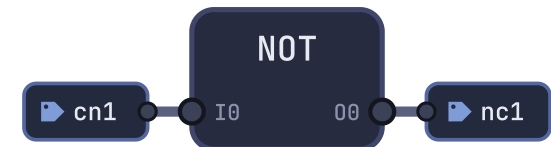
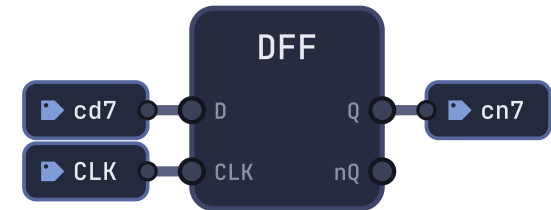
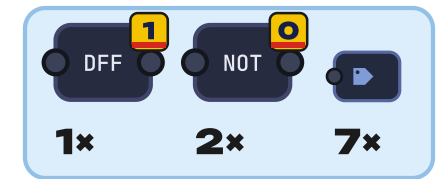
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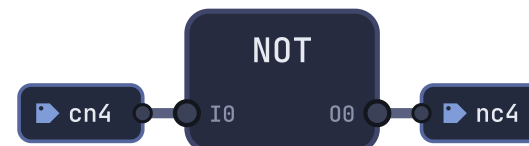
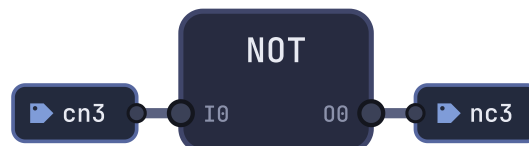
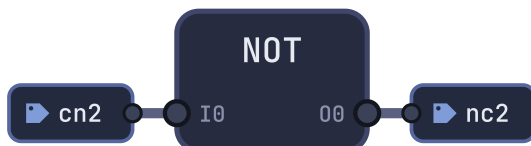
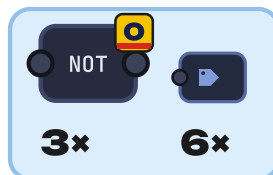
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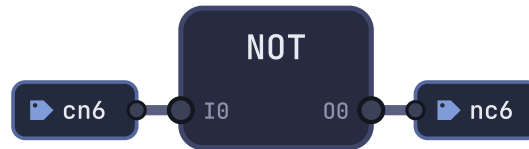
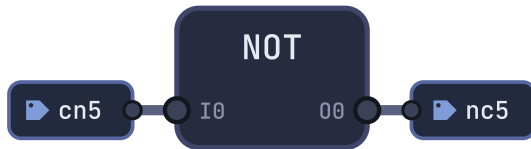
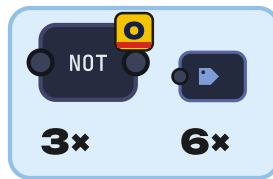
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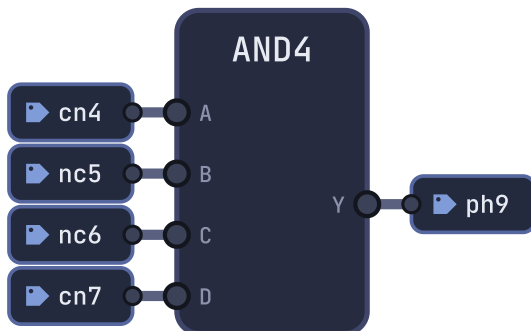
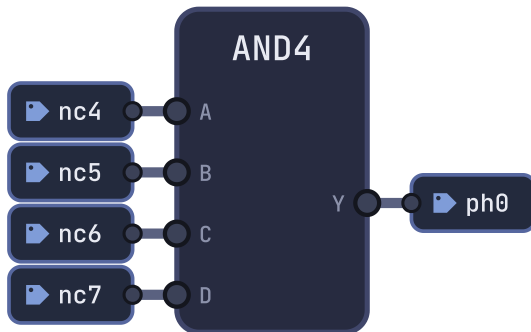
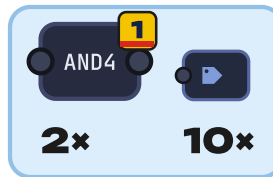
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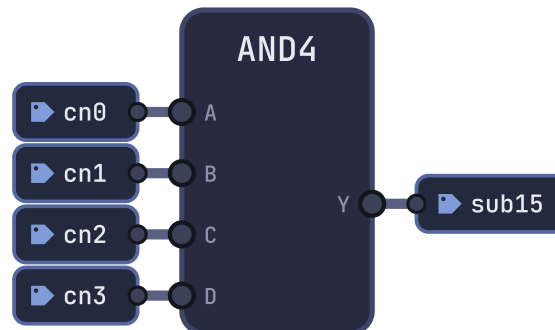
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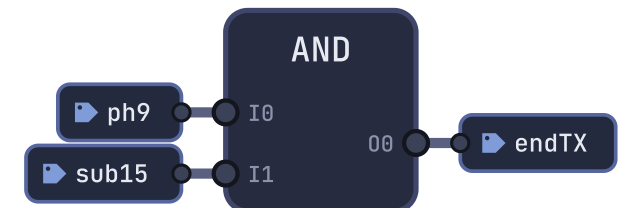
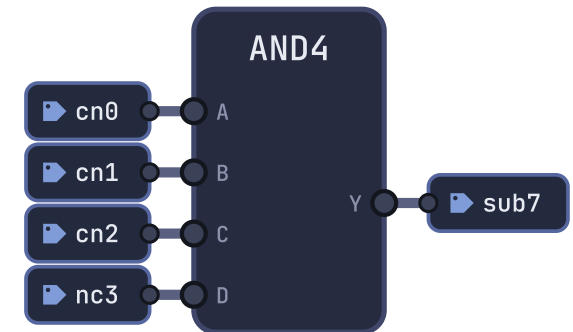
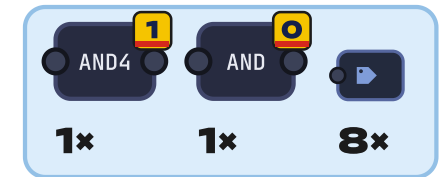
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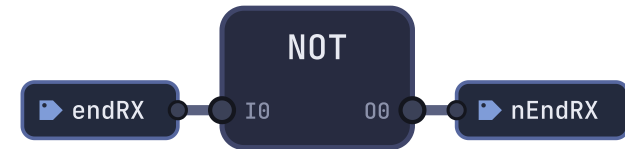
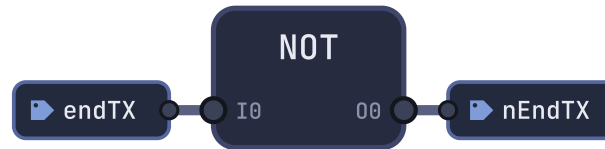
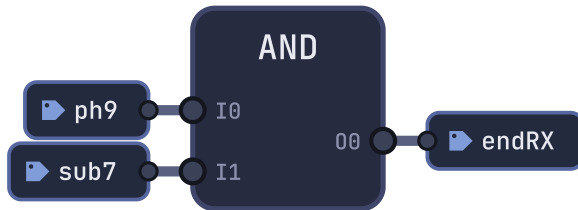
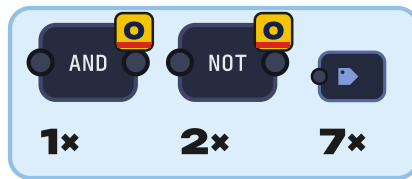
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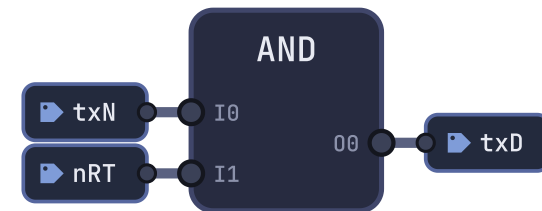
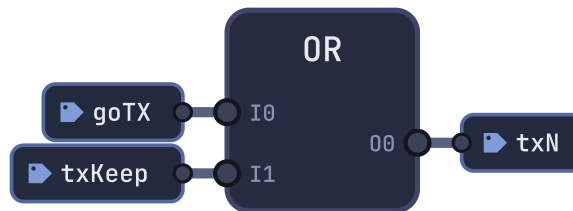
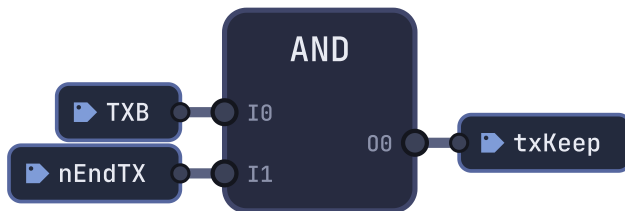
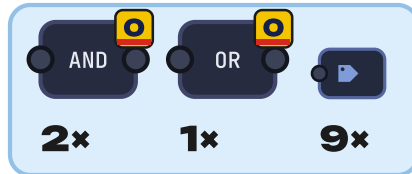
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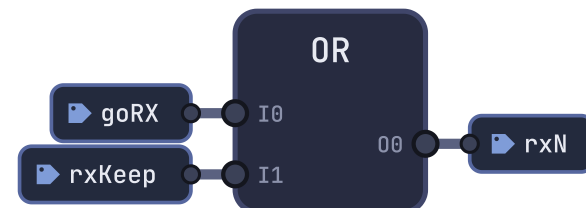
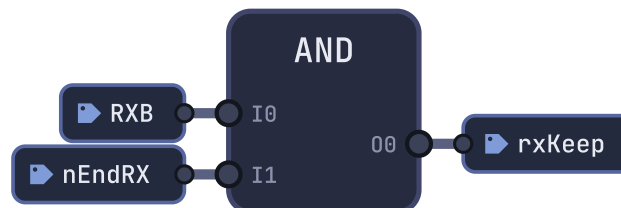
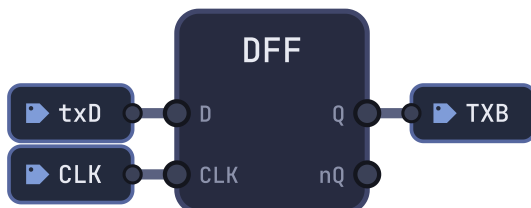
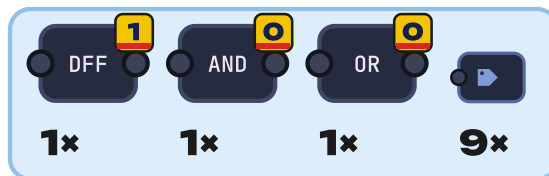
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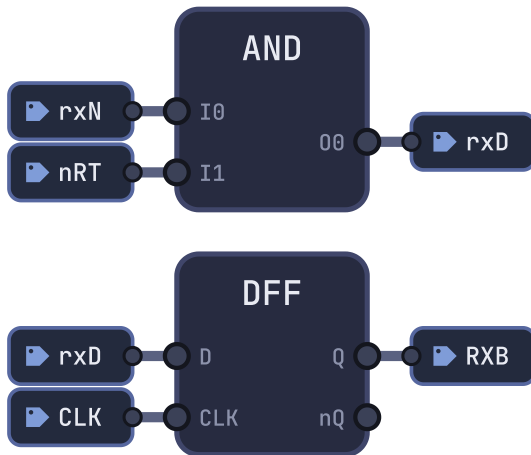
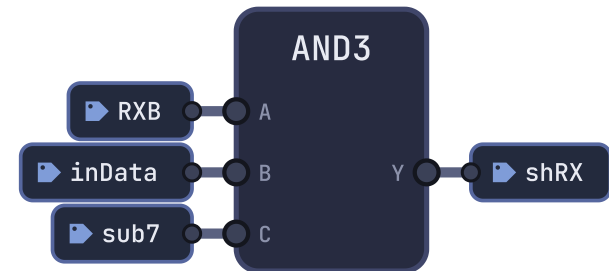
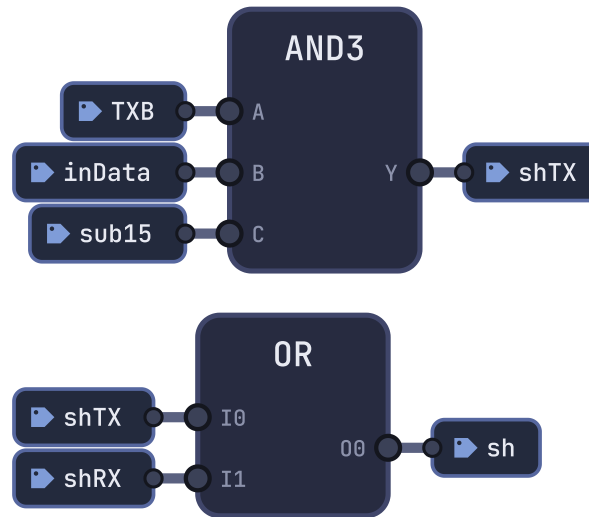
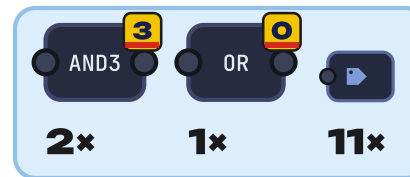
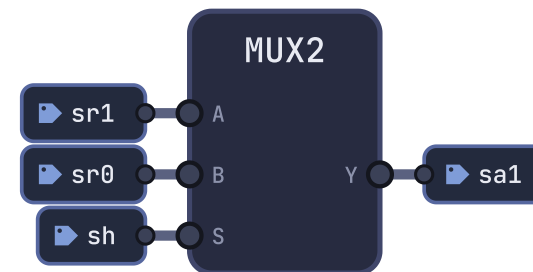
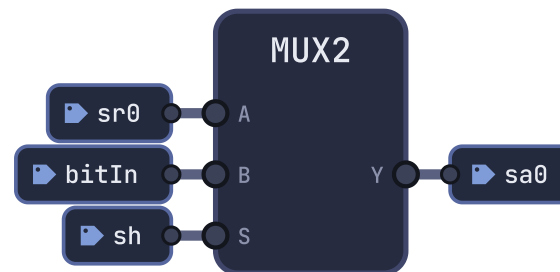
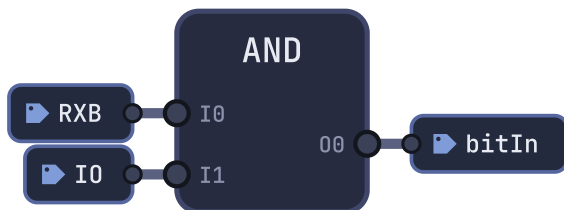


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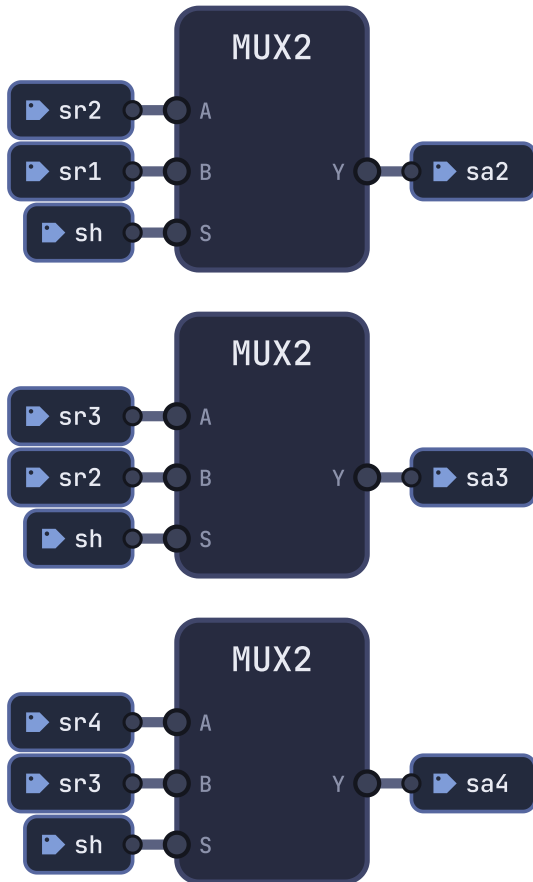


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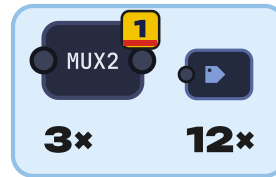


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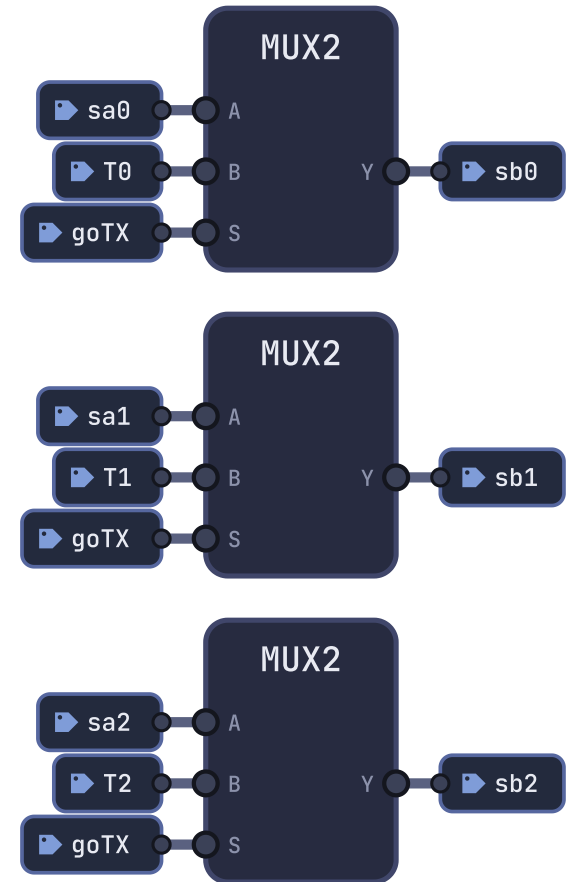
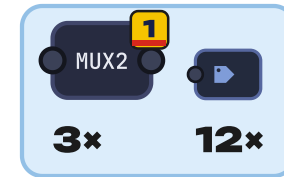
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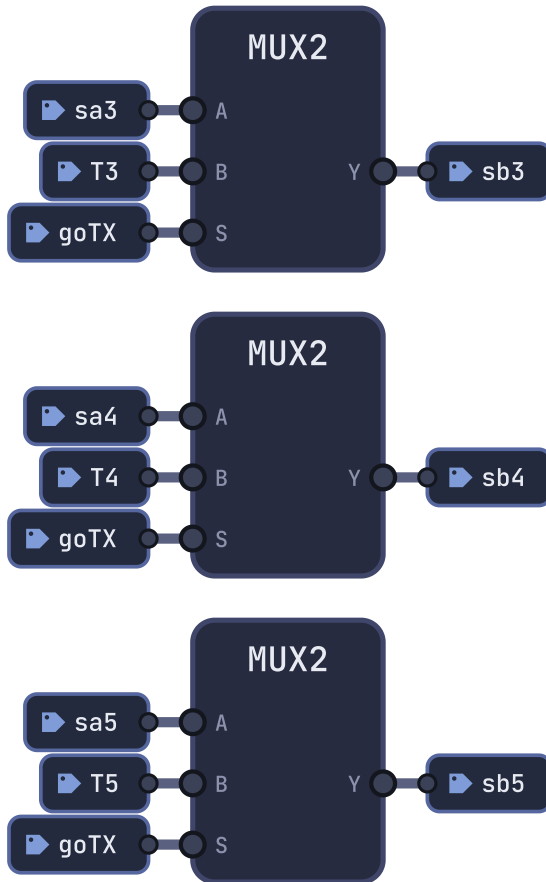
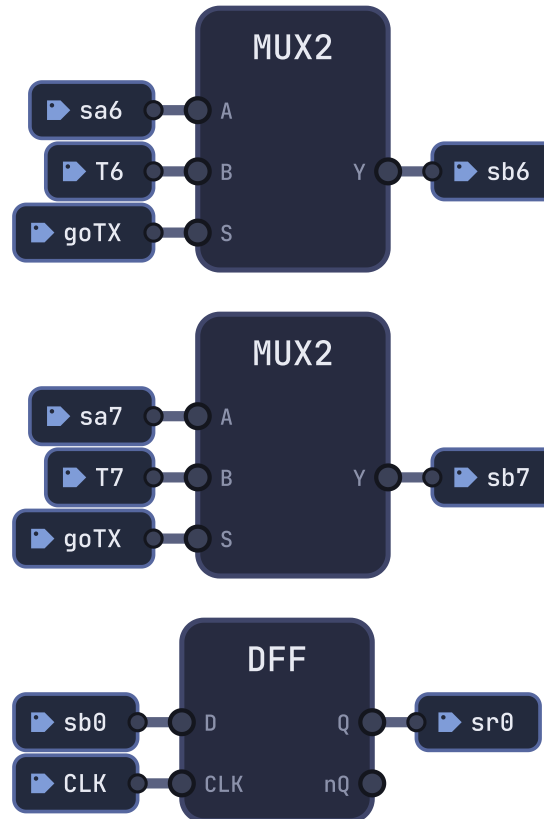
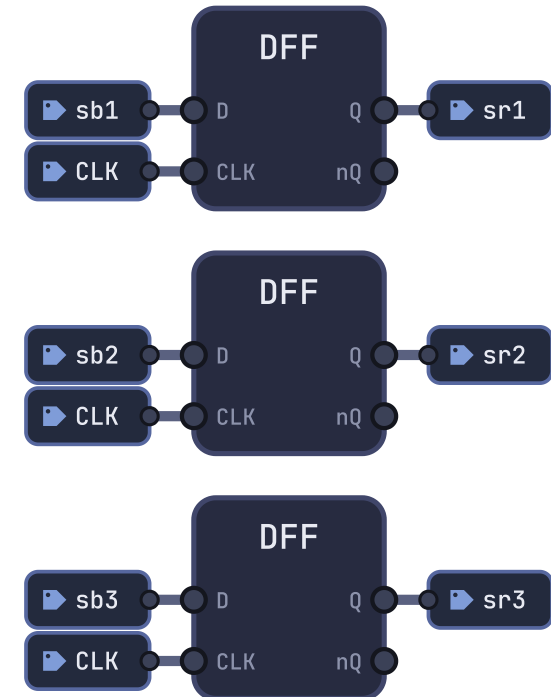
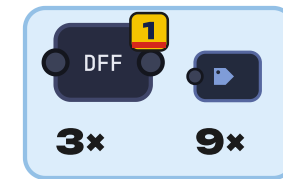


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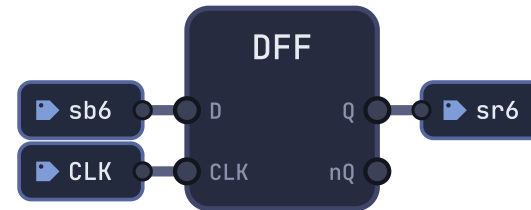
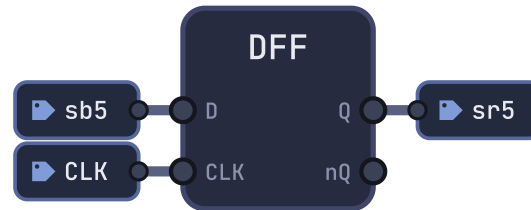
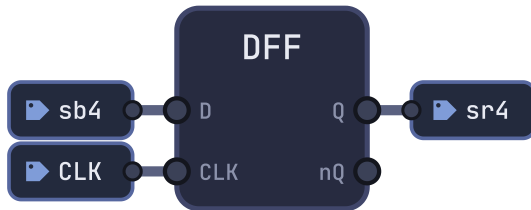


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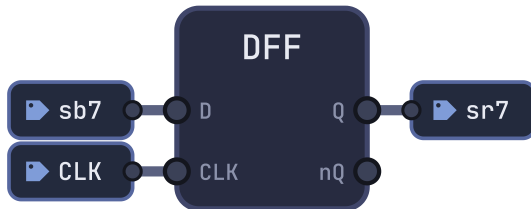


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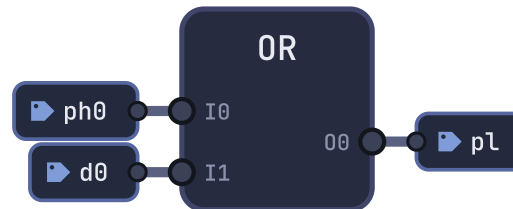
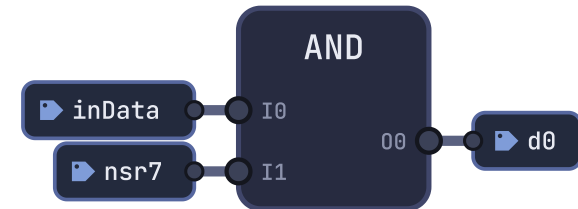
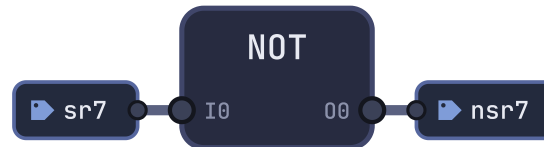
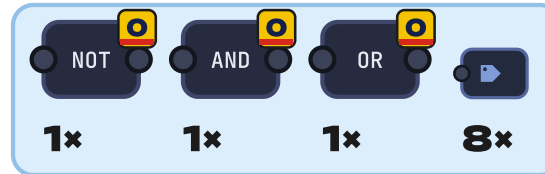
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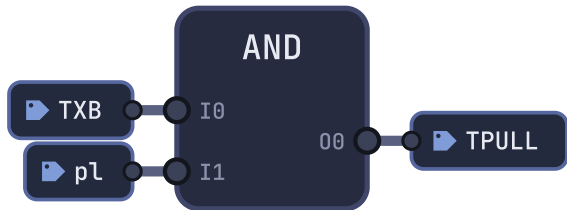
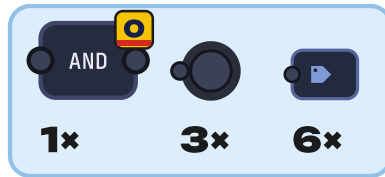
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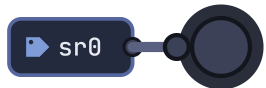
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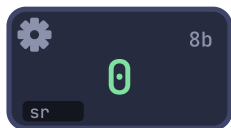
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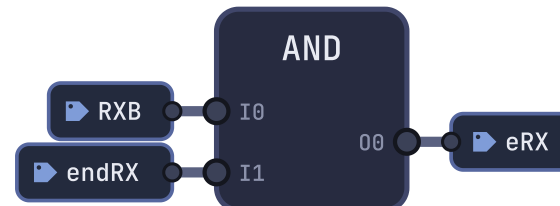
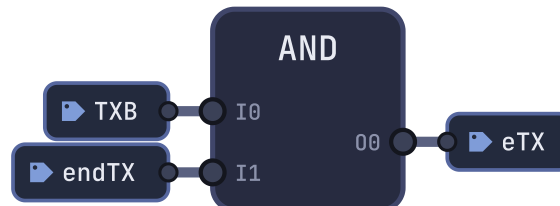
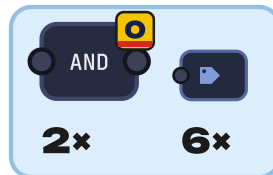
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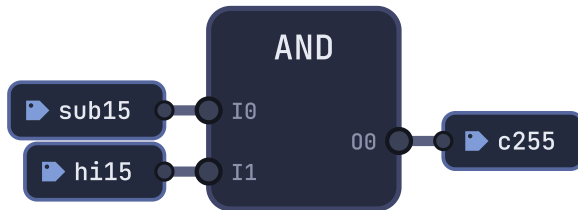
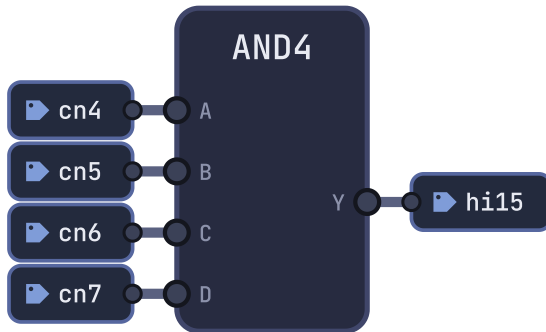
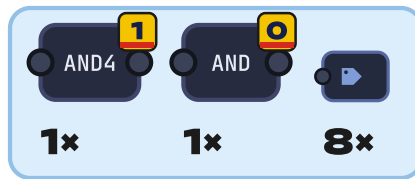
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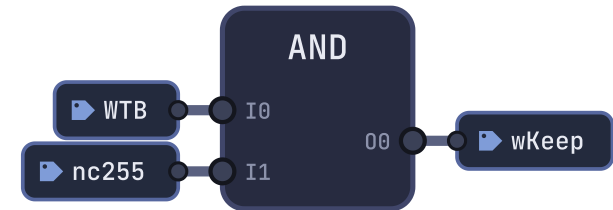
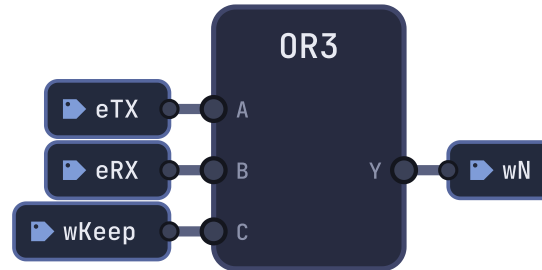
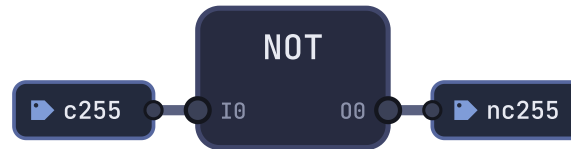
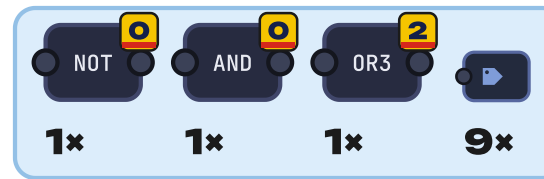
43



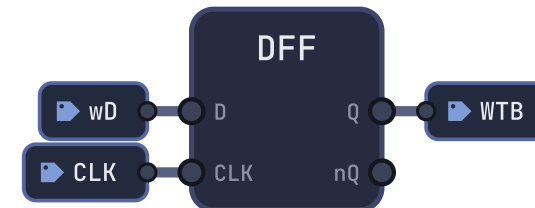
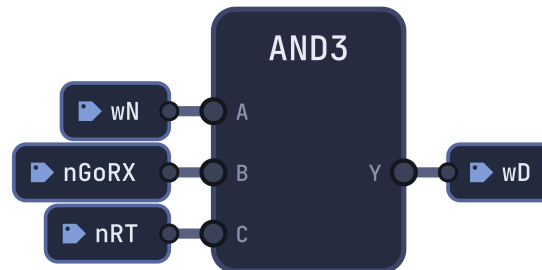
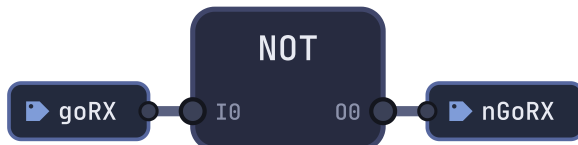
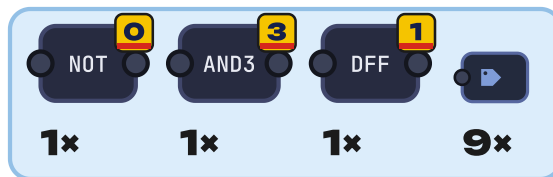
44



45



46



47


1×


1×



48

ROM
256 × 16



Memory
0801 0802 0804
0808 0810 0820
0840 0880 E011



05-echo.rom.json



1
RST

1 → 0 >

0100 0001 \$41

010001

T7T6T5T4T3T2T1T0

SEND

SEND

Lamp

66

65 + 1

1111 1111 \$FF

11111111

T7T6T5T4T3T2T1T0

SEND

SEND

Lamp

0

255 + 1 = 0



Personal data and PIN

kh HT-01

number, PIN and key – in transistors

	pb7	pb6	pb5	pb4	pb3	pb2	pb1	pb0	
pr0								●	01
pr1				●			●		12
pr2			●	●		●			34
pr3		●		●	●		●		5A
pr4	●	●					●	●	C3
pr5				●		●	●	●	17
pr6	●				●	●	●		8E

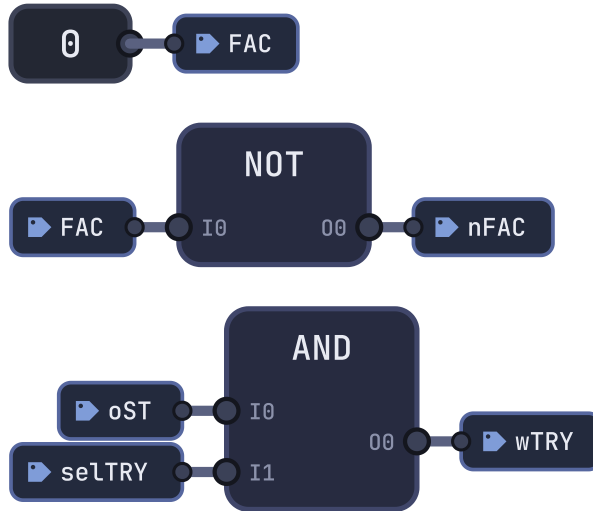
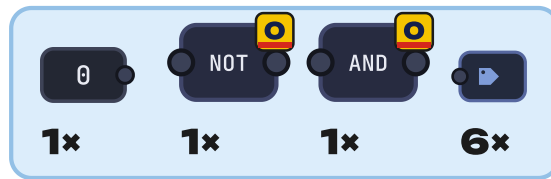
account 01

PIN 12 34

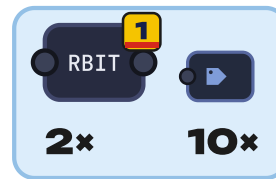
key 5A C3 17 8E



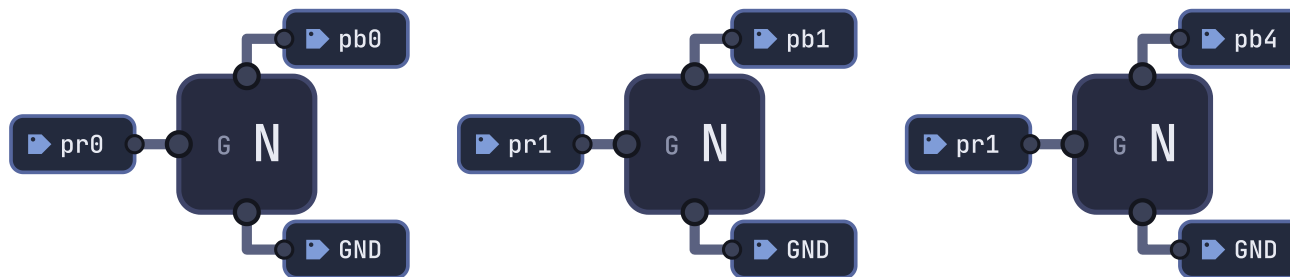
1



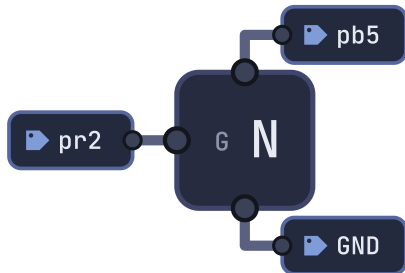
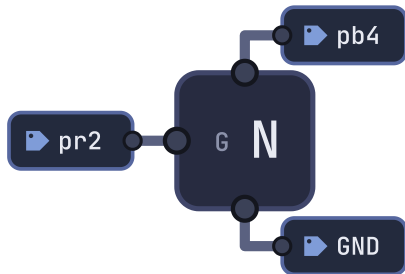
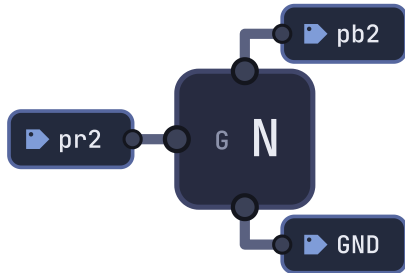
2



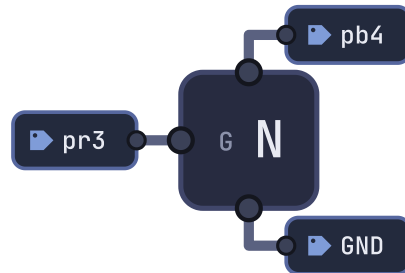
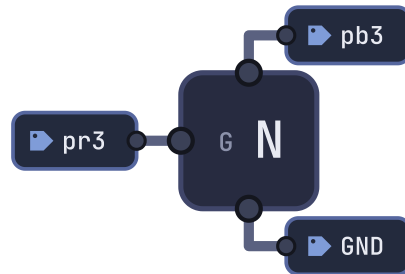
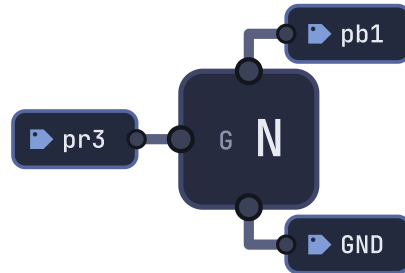
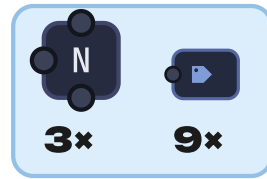
3



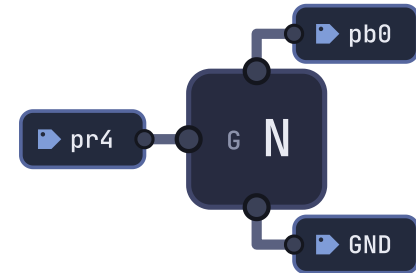
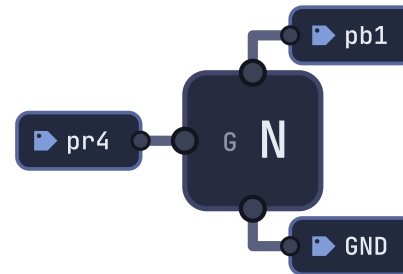
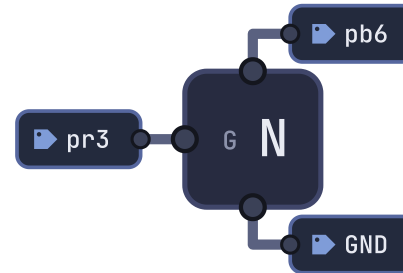
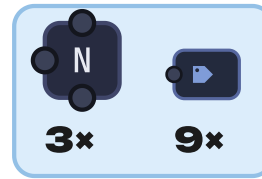
4



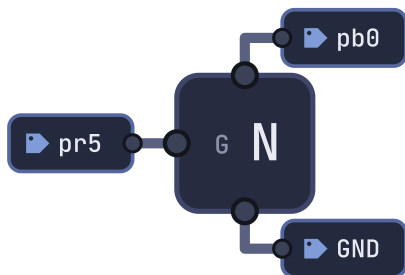
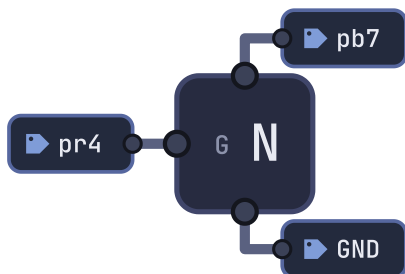
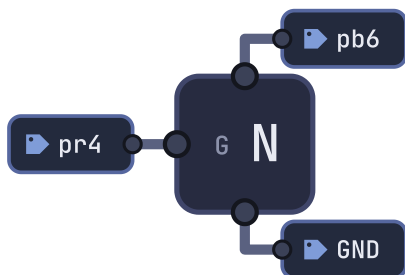
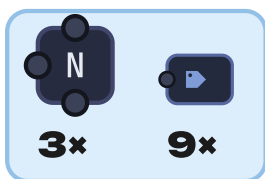
5



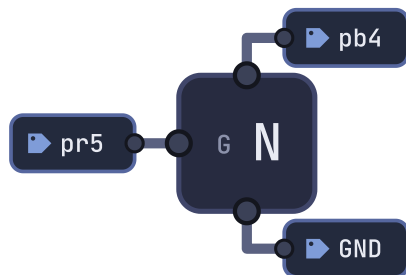
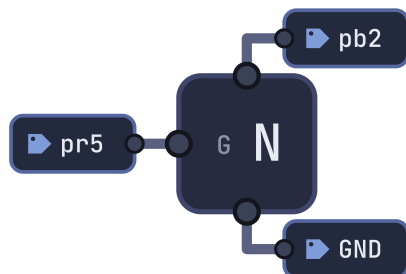
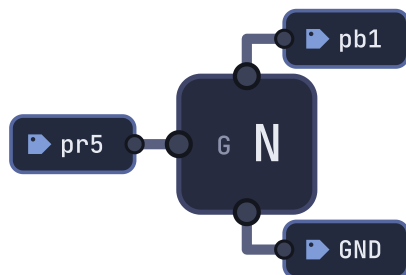
6



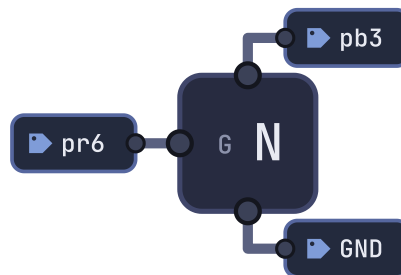
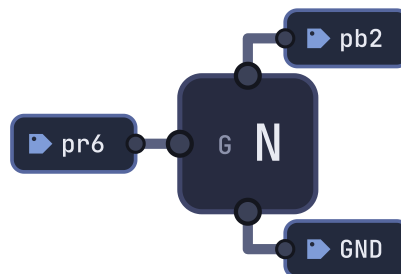
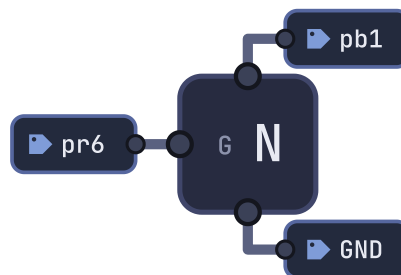
7



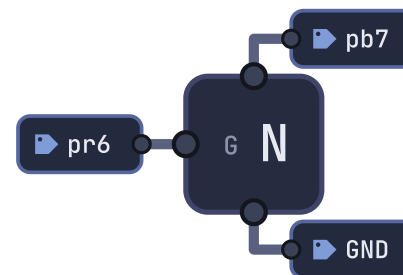
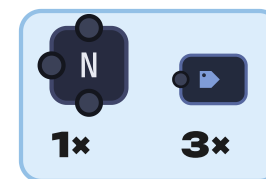
8



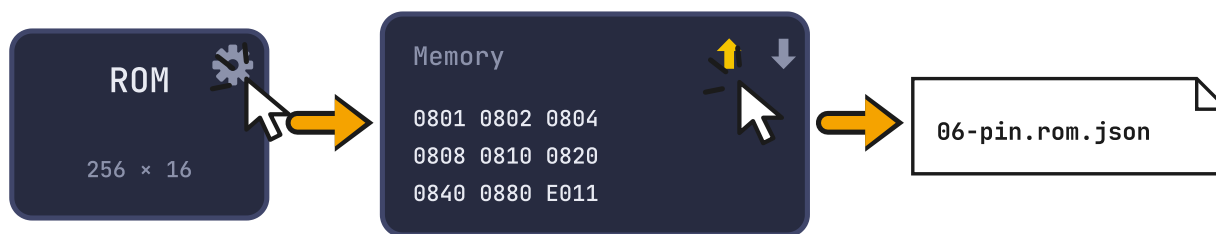
9



10



11



1 1 1 → 0 >

RST FAC

59 \$3B

0100 1110 \$4E

0 1 0 0 1 1 1 0

T7 T6 T5 T4 T3 T2 T1 T0

SEND
SEND

Lamp

1 N

0101 0000 \$50

0 1 0 1 0 0 0 0

T7 T6 T5 T4 T3 T2 T1 T0

SEND
SEND

Lamp

— P

0001 0010 \$12

0 0 0 1 0 0 1 0

T7 T6 T5 T4 T3 T2 T1 T0

SEND
SEND

Lamp

— 12

0011 0100 \$34

0 0 1 1 0 1 0 0

T7 T6 T5 T4 T3 T2 T1 T0

SEND
SEND

Lamp

144 34 → \$90

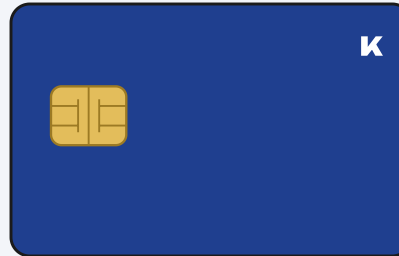


The card program

kh HT-01

challenge → response: the secret never leaves

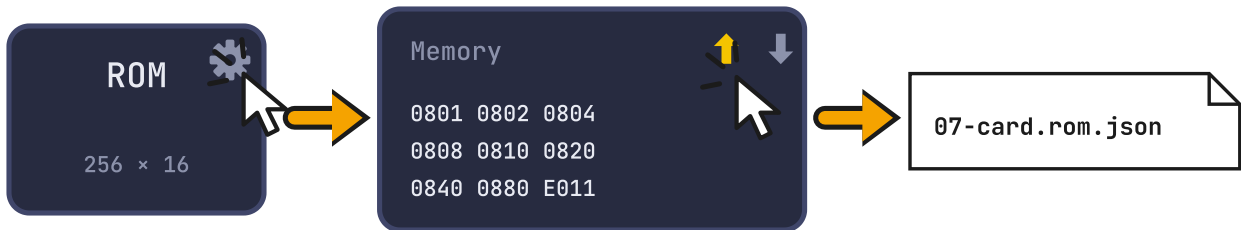
A5 3C



68 F7

$$L \oplus K \cdot H^i = L \cdot \circlearrowleft 1 \times 4$$

1



1 1 → 0 >

59 \$3B

0100 0001 \$41

0 1 0 0 0 0 0 1

SEND SEND

Lamp

—

A

1010 0101 \$A5

1 0 1 0 0 1 0 1

SEND SEND

Lamp

—

A5

0011 1100 \$3C

0 0 1 1 1 1 0 0

SEND SEND

Lamp

105

\$69: no PIN

... P 12 34 → 144

0011 1100 \$3C

0 0 1 1 1 1 0 0

SEND SEND

Lamp

104

A A5 3C → \$68

0101 0010 \$52

0 1 0 1 0 0 1 0

SEND SEND

Lamp

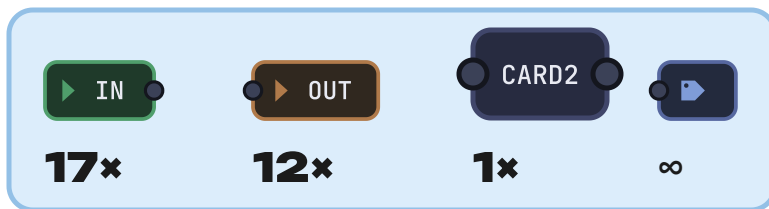
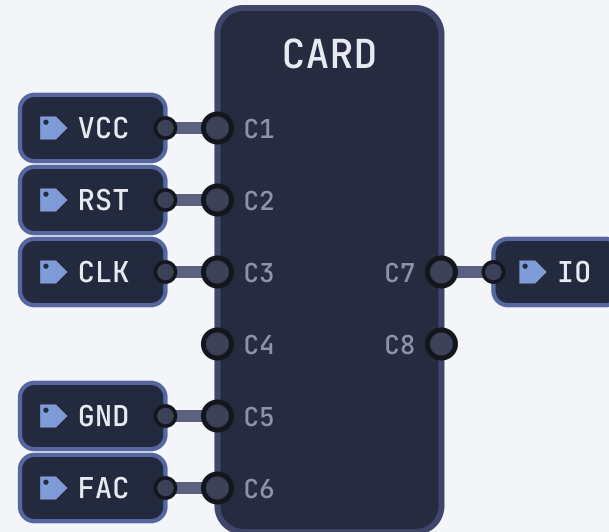
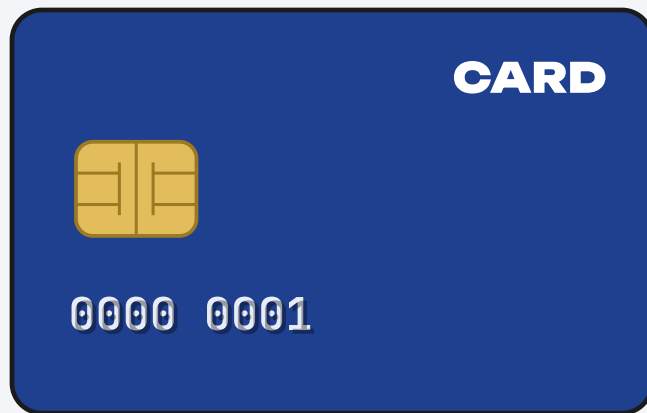
247

R → \$F7



The card as a chip

8 legs, a second card, the tester as a chip too

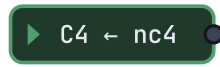
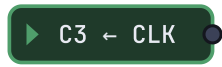


CANVAS

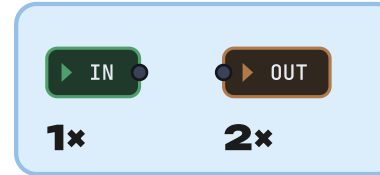
outside: Clock, RST, FAC, the tester, Power, Ground

1

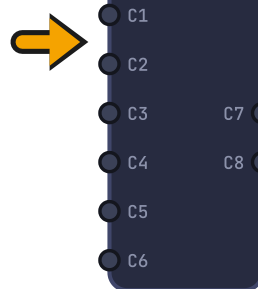
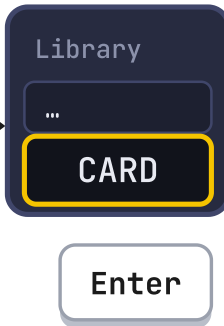
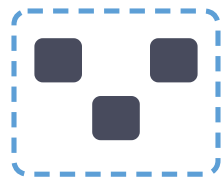
2



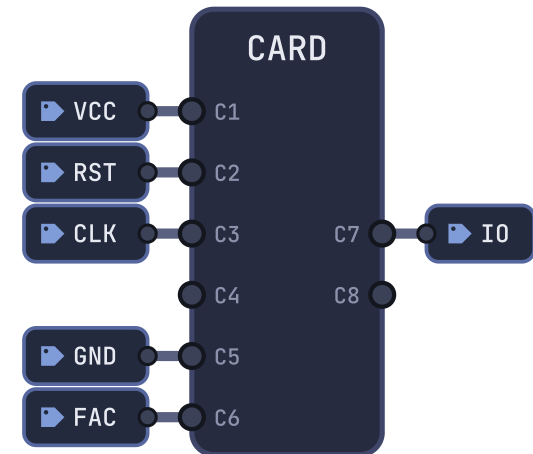
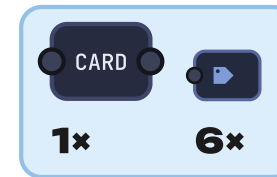
3



4



5



CANVAS ...



1
RST

1
FAC

1 → 0 >

59 \$3B

0100 1110 \$4E

0
T7

1
T6

0
T5

0
T4

1
T3

1
T2

1
T1

0
T0

SEND
SEND

Lamp

1 N → 1

... P 12 34 → 144 · A A5 3C → 104

0101 0010 \$52

0
T7

1
T6

0
T5

1
T4

0
T3

0
T2

1
T1

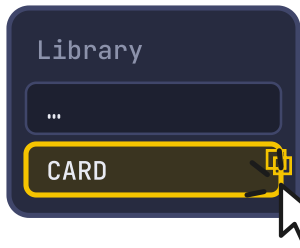
0
T0

SEND
SEND

Lamp

247 R → \$F7

6



Enter

copy of the chip

7

Edit → matrix pr0-pr6 × pb7-pb0

	pb7	pb6	pb5	pb4	pb3	pb2	pb1	pb0	
pr0							+	×	01 → 02
pr1		+		×			●	+	12 → 43
pr2			●	×		×		+	34 → 21
pr3		×	+	×	×		×	+	5A → 21
pr4	●	×		+	+	+	●	●	C3 → 9F
pr5	+	+	+	×		●	×	×	17 → E4
pr6	×		+	+	●	×	●	+	8E → 3B

● there, keep

× remove

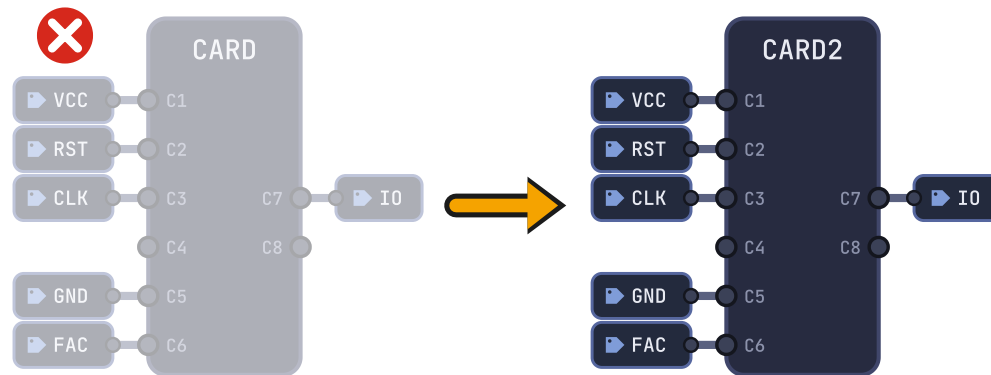
+ add: nmos(pr, pb, GND)

□ empty

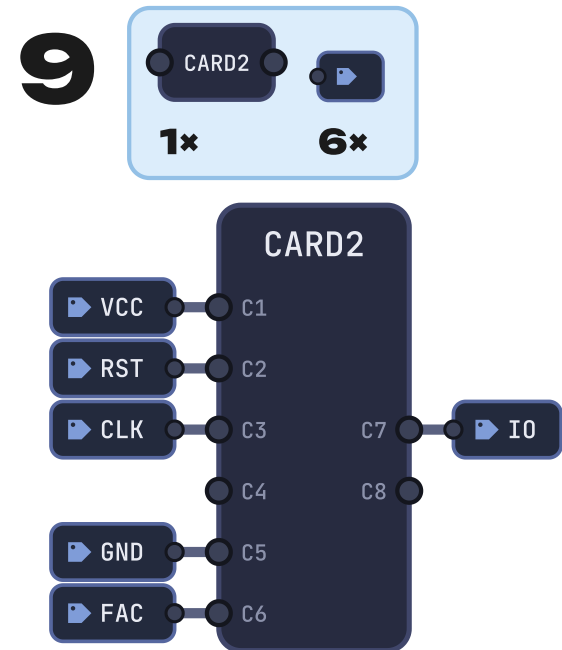
remove 14 • add 15 • keep 8

8

take out CARD – insert CARD2: the same 6 labels on the same legs



9



CANVAS ...



Diagram illustrating the bit values for T7 through T0:

Bit	T7	T6	T5	T4	T3	T2	T1	T0
Value	0	1	0	0	1	1	1	0



➤ ●●●●●●●● **2** N → 2

Diagram illustrating the bit pattern for the value 10100100 (decimal 164) stored in an 8-bit register. The bits are labeled T7 through T0 from left to right. The bit values are: T7=0, T6=1, T5=0, T4=1, T3=0, T2=0, T1=1, T0=0.

Bit	T7	T6	T5	T4	T3	T2	T1	T0
Value	0	1	0	1	0	0	1	0



> ●●●●●●● **221** R → \$DD

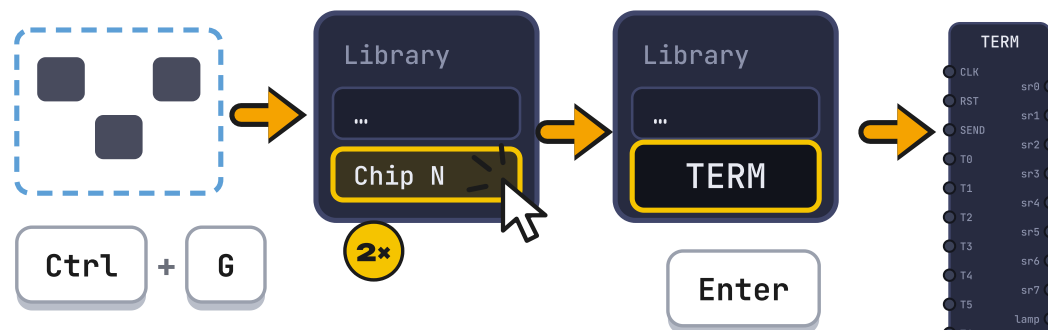
switches, SEND, lamps and display stay outside

IN 11x

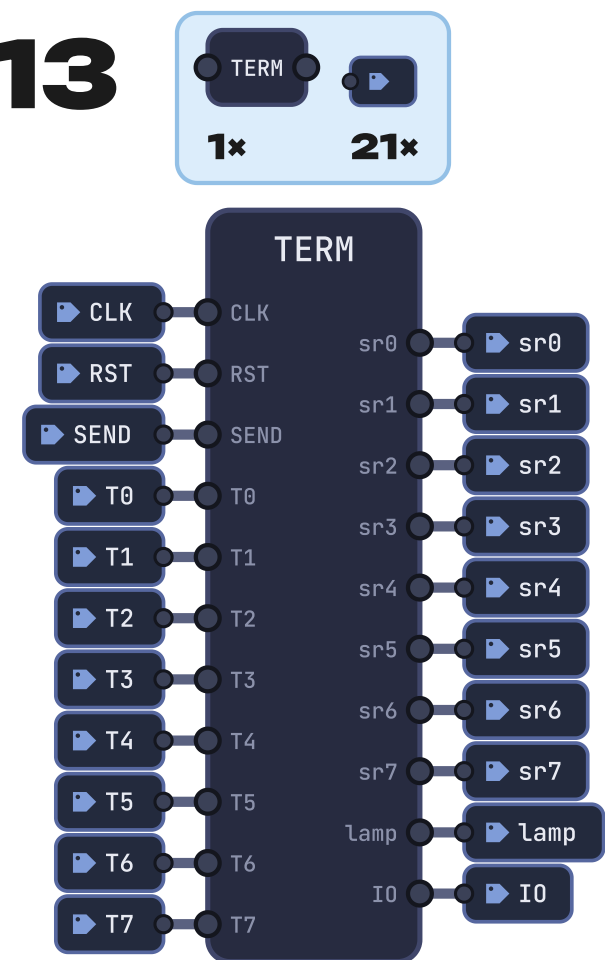
OUT 10x



12



13



Kit parts

how many times you place each part over all the lessons



35×



11×



9×



2×



2×



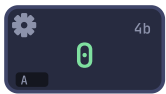
22×



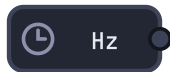
19×



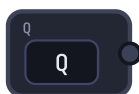
1×



3×



1×



2×



85×



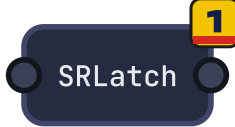
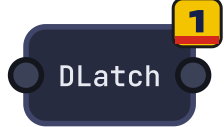
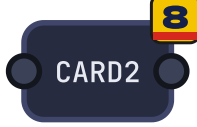
67×



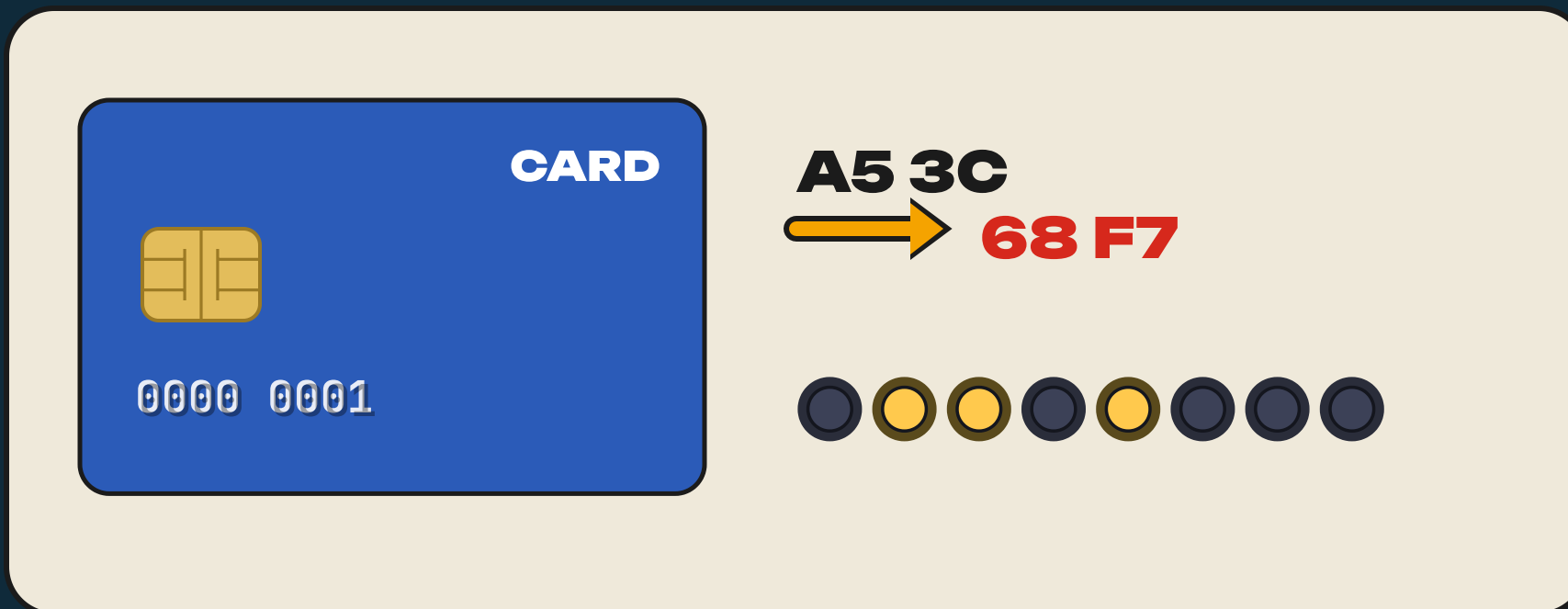
1917×

Kit chips

you build them yourself: each one is made of the ones before

 OR 32×	 NAND 4×	 AND 92×	 NOR 4×	 NOT 47×	 XOR 19×	 SRLatch 1×	 DLatch 10×
 MUX2 73×	 DFF 30×	 OR4 4×	 AND4 21×	 DEC16 1×	 FA 8×	 RBIT 21×	 OR8 9×
 HA 14×	 OR3 5×	 AND3 16×	 DEC8 1×	 WORD8 8×	 CARD 1×	 CARD2 1×	 TERM 1×

Done!



a card of 6,495 transistors answers the tester's challenge

insert CARD2 – the same program, other transistors, another answer

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HT-01